



# Tailoring the Crystallographic Texture and Electrical Properties of Inkjet-printed Interconnects for Use in Microelectronics

Romain Cauchois, Mohamed Saadaoui, Karim Inal, Béatrice Dubois-Bonvalot, Jean-Christophe Fidalgo

## ► To cite this version:

Romain Cauchois, Mohamed Saadaoui, Karim Inal, Béatrice Dubois-Bonvalot, Jean-Christophe Fidalgo. Tailoring the Crystallographic Texture and Electrical Properties of Inkjet-printed Interconnects for Use in Microelectronics. Materials Research Society Spring Meeting, 2011, San Francisco, United States. 1323, pp.O8.10, 2011, <10.1557/opl.2011.1264>. <emse-00576968>

**HAL Id: emse-00576968**

**<https://hal-emse.ccsd.cnrs.fr/emse-00576968>**

Submitted on 3 Oct 2012

**HAL** is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers.

L'archive ouverte pluridisciplinaire **HAL**, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.

## Tailoring the Crystallographic Texture and Electrical Properties of Inkjet-printed Interconnects for Use in Microelectronics

Romain Cauchois<sup>1,2</sup>, Mohamed Saadaoui<sup>2</sup>, Karim Inal<sup>2</sup>, Beatrice Dubois-Bonvalot<sup>1</sup> and Jean-Christophe Fidalgo<sup>1</sup>

<sup>1</sup>Innovation and Manufacturing Technologies Department, Gemalto, 13881 Gemenos, FRANCE

<sup>2</sup>Centre Microelectronique de Provence, Ecole Nationale Supérieure des Mines de Saint-Etienne, 880 avenue de Mimet 13541 Gardanne, FRANCE

### ABSTRACT

In this paper, silver nanoparticles with a mean diameter of 40 nm are studied for future applications in microelectronic devices. The enhanced diffusivity of nanoparticles is exploited to fabricate electrical interconnects at low temperature. Sintering condition has been tuned to tailor the grain size so that electrical resistivity can be lowered down to 3.4  $\mu\text{Ohm}\cdot\text{cm}$ . In this study, a  $\{111\}$ -textured gold thin film has been used to increase diffusion routes. The combined effects of the substrate crystalline orientation and the sintering condition have been demonstrated to have a significant impact on microstructures. In particular, a  $\{111\}$  fiber texture is developed above 300°C in printed silver only if the underlying film exhibits a preferential orientation. This condition appeared as essential for the efficiency of the gold wire-bonding process step. Thus, inkjet-printed interconnects show a prospective potential compared to conventional subtractive technique and offers new opportunities for low cost metallization in electronics packaging.

### INTRODUCTION

Additive printing technologies have gained tremendous interest as a pathway to large area and flexible electronics. Among several printing methods, drop-on-demand inkjet printing is a non contact and digital technique that allows fast prototyping without any waste. This technology can thus be advantageously adapted for the realization of interconnects on silicon ICs for low cost electronic packaging [1]. Those interconnects are patterned by jetting a colloidal suspension of metal nanoparticles whose thermodynamic size effect is exploited to reduce the sintering temperature [2,3]. Printed features should exhibit a low electrical resistivity and high mechanical properties for being compatible with subsequent wire bonding step. Tuning those physical properties are particularly challenging since an optimization of microstructure through a solid-state sintering is required. Hence, a proper IC compatible post-process using a well-timed temperature profile has to be properly adjusted.

Electrical conduction of patterns is thermally activated both by the evaporation of solvents and by the sintering of metallic nanoparticles. Sintering is a complex physical phenomenon which operates as soon as solvents are evaporated to cast bonds between particles. Amongst mechanisms, surface diffusion, grain boundary diffusion and lattice diffusion are dominant in nanoparticles. Since a large stress is required for plastic flow in a nanoparticulate system, it is believed that dislocation-driven plastic flow is unlikely to be a major contributor to neck growth in face-centered cubic nanoparticles [4]. In addition to their increased curvature, nanoparticles include unique defect structures (twins and facets) and enhanced diffusivity due to

the size effect that lowers the sintering temperature far below predictions of scaling models.

Even though Ag/Au heterodiffusion is well-known for bulk materials [5], the behavior of nanoparticles on thin films remains scarcely treated still [6]. In this paper, the thermodynamic size effect of silver nanoparticles is studied on both amorphous and on {111}-textured gold layer and wire-bonding process step is evaluated for both printed substrate.

## EXPERIMENTAL DETAILS

An in-line inkjet printer prototype developed in the lab, called JetPac, was employed to pattern the test vehicle. This fully automated prototype allows sequential pre-treatment and post-processing of printed substrate to implement an industrial roll-to-roll process. The drop-on-demand inkjet system operates by propelling 30 pL droplets through nozzles. Inkjet process parameters such as the bipolar waveform, meniscus and droplets ejection velocity have been finely tuned to achieve high resolution patterns and defect free interconnects.

Silver colloids with a mean diameter of 40 nm were inkjet-printed on top of a {100} silicon substrate. This silicon is coated with either amorphous silicon nitride or with gold thin film. The 580 nm thick  $\text{Si}_3\text{N}_4$  layer is prepared by Plasma-Enhanced Chemical Vapor Deposition (PECVD), and the 50 nm / 200 nm thick Ti/Au bilayer is prepared by thermal evaporation at nominal room temperature. Silver printed patterns were consecutively sintered in a Rapid Thermal Annealing (RTA) oven within a temperature range of 200°C to 500°C, during 15 min, and using a ramp of 10°C/s. The thickness of the printed silver thin film is measured between 0.4 and 1  $\mu\text{m}$  and electrical resistivity is measured with a four-point probe equipment.

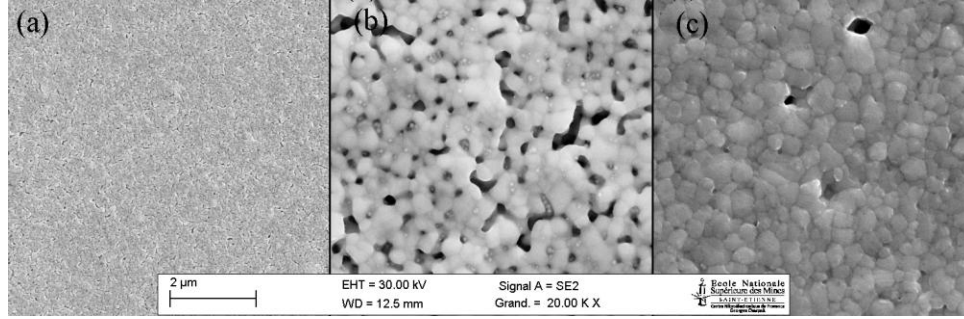
The crystallographic texture and the grain size of those printed silver films have been investigated using Electron Back-Scattered Diffraction (EBSD) in a FEG-SEM operated at 30 kV. Orientation maps were performed on a 40x40  $\mu\text{m}^2$  square window with a step size of 50 nm. A binning of 4x4 and a minimum of 5 bands was chosen for pattern identification.

The wire-bonding process was performed on an ESSEC 3100 with a 25  $\mu\text{m}$  gold wire. The melted gold ball is formed by a 150 mA Joule heating current, while the metallurgical weld between the free-air ball and the pad is casted with a 350 mN bonding force during 7 ms.

## RESULTS AND DISCUSSION

### Correlation of grain size and electrical resistivity

During the sintering process, the neck growth occurs simultaneously with a grain growth resulting in a film densification and a reduction of pores density. According the sintering process (temperature, time, ramp and atmosphere), microstructure of the printed silver nanoparticles can thus be tailored to reach an optimal electrical resistivity. Figure 1 shows a SEM view of thin silver film surface morphology after being sintered on gold substrate at different temperature.



**Figure 1.** SEM images of inkjet-printed film surfaces sintered respectively at 200°C (a), 300°C (b) and 500°C (c) on evaporated gold layer.

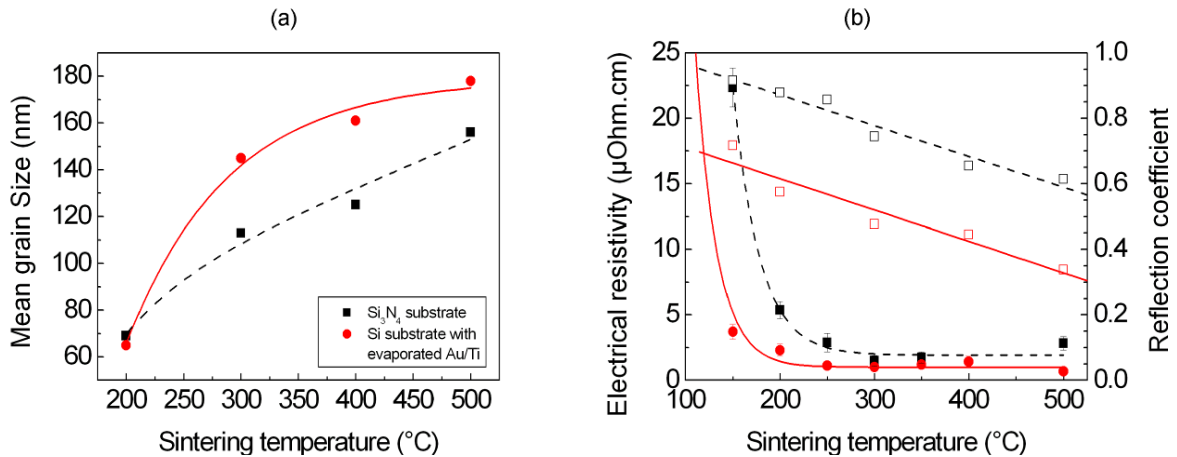
In thin films, electrons undergo multiple scattering from the surface and grain boundaries, which depend on film thickness and grain size respectively. Indeed, according previous work from Mayadas and Shatzkes [7], grain boundary enhanced electrical resistivity  $\rho_{gr}$  is given by:

$$\rho_{gr}(T) = \rho_{\infty}(T) \left[ 1 - \frac{3}{2}\alpha + 3\alpha^2 - 3\alpha^3 \ln \left( 1 + \frac{1}{\alpha} \right) \right]^{-1} \quad (1)$$

$$\alpha = \frac{\lambda_{\infty}(T)}{G} \frac{R}{1-R} \quad (2)$$

where  $\rho_{\infty}(T)$  is the bulk resistivity at temperature T; G is the average grain diameter; R is the reflection coefficient of electrons diffusely scattered at grain boundaries ( $0 \leq R \leq 1$ );  $\lambda_{\infty}(T)$  is the electron mean free path in the bulk material.

Electrical resistivity can thus be lowered drastically by tailoring the morphology of printed thin films. SEM images were processed by a routine in an image analysis software (NIH ImageJ). The average grain size is plotted for both substrates according sintering conditions in Figure 2. Additionally, reflection at grain boundaries is plotted together with the resistivity according Equation 1 and 2 to better assess the quality of grain boundary mismatch.

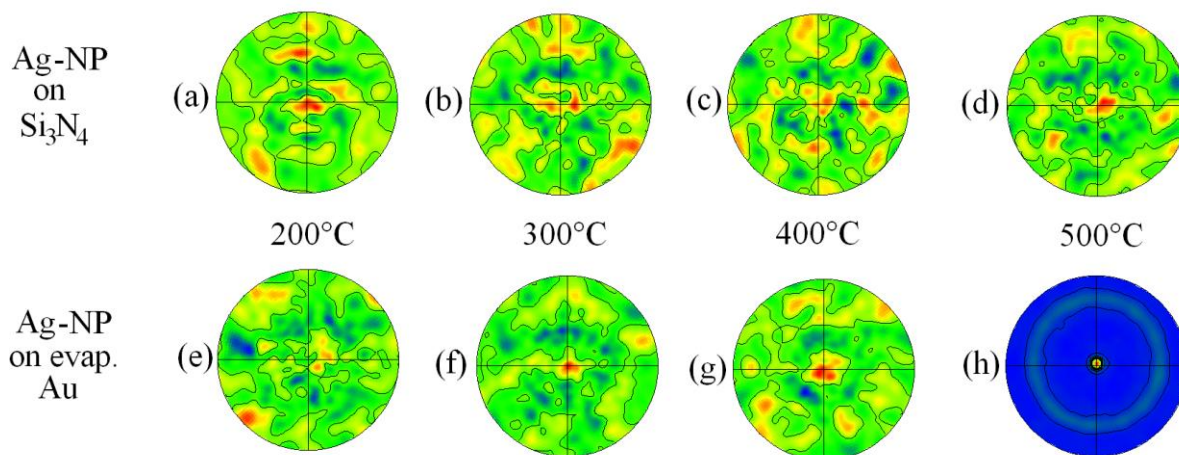


**Figure 2.** Average silver grain size (a) with the evolution of electrical resistivity (solid symbols) and reflection coefficient (plain symbols) (b) on either Si<sub>3</sub>N<sub>4</sub> (dashed black line) or evaporated Au/Ti layer (solid red line).

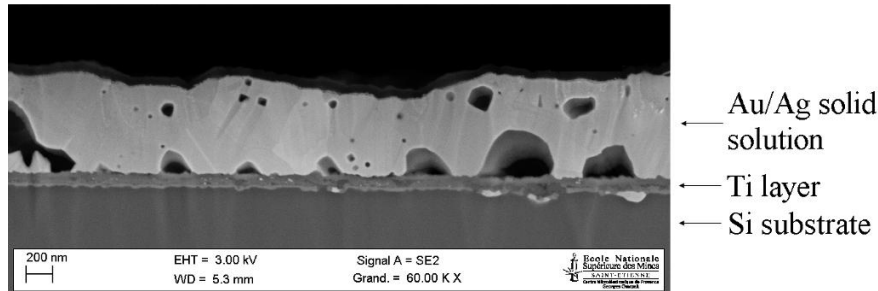
As expected, the mean grain size as well as the electrical resistivity of silver nanoparticles shows a strong dependency to sintering temperature. Note that the heating rate has been previously optimized and the  $10^{\circ}\text{C}/\text{s}$  ramp exhibits a good compromise between electrical and mechanical properties [8]. Moreover, the mean grain size of nanoparticles is clearly affected by the underlying layer as shown in Figure 2a. At  $200^{\circ}\text{C}$ , surface morphologies of printed films are similar due to the fact that neck growth occurs between nanoparticles themselves as well as between nanoparticles and the underlying surface. Electrically, the resistivity of sintered silver on silicon nitride is twice as much as on gold substrate, meaning that the contact resistance and the grain boundary reflection between silver and gold are quite low even at  $200^{\circ}\text{C}$  (see Figure 1b). Above  $200^{\circ}\text{C}$ , the mean grain size of silver nanoparticles on textured gold substrate is more pronounced, which indicates that nanoparticles sintering is still occurring and that it is assisted by Au/Ag interdiffusion. This interdiffusion tends to decrease the overall electrical resistivity by reducing the Au/Ag contact resistance, and a value of  $2\mu\text{Ohm}\cdot\text{cm}$  can be achieved.

### Sintering-assisted interdiffusion between silver NP and gold substrate

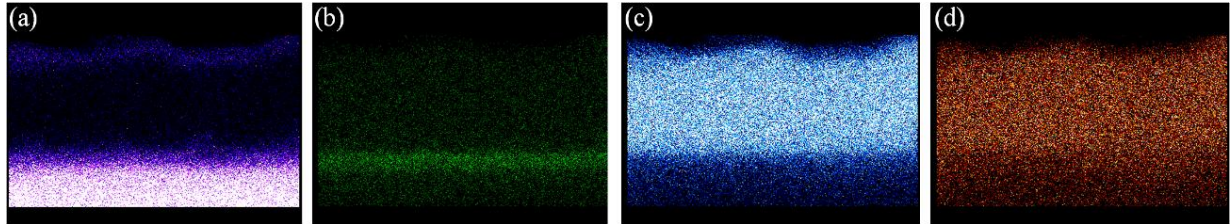
In FCC metals, surface energy minimization promotes the growth of  $\{111\}$  grains while strain energy minimization is supporting  $\{100\}$  grain growth [9]. It is commonly accepted that surface energy minimization is dominant in polycrystalline thin films, leading to a preferential  $\{111\}$  orientation when those films are thermally cured. For silver nanoparticles, at initial sintering stage, the surface energy minimization tends to promote the neck growth before any thermal activation of Ostwald ripening phenomenon, leading to coarse grains. This last step is promoting  $\{111\}$  crystallographic texture. Figure 3a-d displays the pole figures of sintered silver nanoparticles on amorphous silicon nitride. The activation energy for  $\{111\}$  texturation is achieved at  $500^{\circ}\text{C}$  when a  $\{111\}$  pole is emerging. However, for silver nanoparticles being sintered on textured gold substrate, this activation energy is reached as low as  $300^{\circ}\text{C}$  because of the driving energy supplied by out-of-plane interdiffusion of gold into silver (see Figure 3e-h). This Ag/Au system is totally miscible throughout the whole range composition. Figure 4 shows a SEM and EDX cross-section views of Au/Ag solid solution after being sintered at  $500^{\circ}\text{C}$ .



**Figure 3.**  $\{111\}$ -pole figures of inkjet-printed silver nanoparticles film on a silicon nitride substrate (a-d) and on  $\{111\}$  evaporated gold substrate (e-h) sintered at  $200^{\circ}\text{C}$  (a, e),  $300^{\circ}\text{C}$  (b, f),  $400^{\circ}\text{C}$  (c, g) and  $500^{\circ}\text{C}$  (d, h) with a ramp of  $10^{\circ}\text{C}/\text{s}$  during 15 min under  $\text{N}_2$  atmosphere.



**Figure 4.** SEM image of the Ag/Au/Ti/Si film cross section after ion polishing.



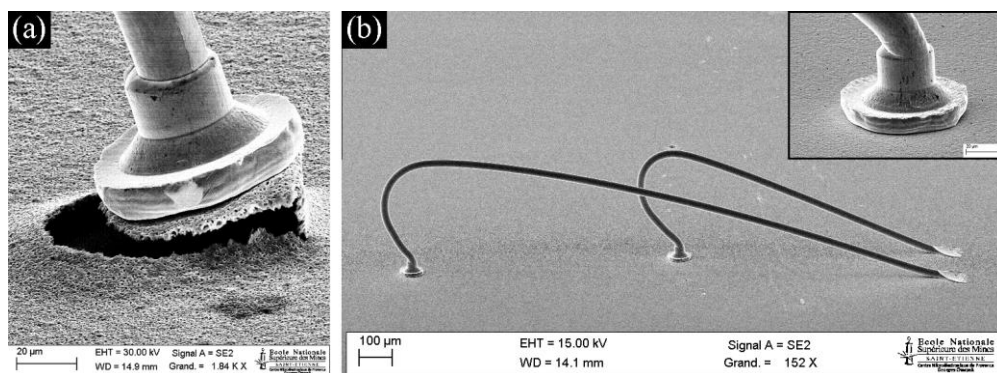
**Figure 5.** EDX mapping of  $K\alpha_1$  of Si (a),  $K\alpha_1$  of Ti (b),  $L\alpha_1$  of Ag and  $M\alpha_1$  of Au.

To further decrease the interdiffusion initiation temperature between textured substrate and nanoparticles-based thin films, one approach consists in reducing those nanoparticles size to few nanometers. Indeed, as previously explained, a nanoparticle diameter shrink entails a decrease of the sintering temperature because of the surface to volume ratio. In parallel, the coefficient of diffusion is size dependent as shown in Equation 3 [10]:

$$D(r, T) = D_0 \exp \left[ \frac{-E(\infty)}{\Re T} \exp \left( \frac{2S_{vib}(\infty)}{3\Re(1 - G/G_0)} \right) \right] \quad (3)$$

where  $D_0$  is a constant,  $E(\infty)$  the bulk activation energy,  $S_{vib}(\infty)$  the bulk melting entropy,  $G$  the particle diameter,  $G_0=3x$  atomic diameter,  $\Re$  the ideal gas constant and  $T$  the temperature.

The impact of crystallographic texture of sintered silver has been further analyzed by ink-jetting interconnection lines and bond pads. Only the  $\{111\}$ -textured silver pads above  $200^\circ\text{C}$  provides perfect gold-wire bondability with a high bonding strength through the increase of both interfacial adhesion and hardness (see Figure 6).



**Figure 6.** Ball-bonding performed failingly on non-textured silver thin film (a) and successfully on textured silver thin film (b) with standard 25  $\mu\text{m}$  gold wire.

The success of the wire-bonding process step is due to the increased hardness of the textured polycrystalline layer. Indeed, the  $\langle 111 \rangle$  direction corresponds to close packed planes in FCC materials with higher Young's modulus:  $E_{\langle 111 \rangle} > E_{\langle 101 \rangle} > E_{\langle 100 \rangle}$ . The residual porosities allow enough mechanical accommodation through deformation during the impact of the ball bonding. Using a  $\{111\}$  fiber-textured thin film underneath an inkjet-printed film thus allows a sufficient film rigidification with an accommodation layer as required by wire bonding process.

## CONCLUSIONS

In this paper, the texture and electrical properties of printed silver nanoparticles is investigated. This texture shows a strong link to the underneath layer. A  $\{111\}$  fiber texture is obtained for films being printed on textured gold layer, and both solid state sintering and interdiffusion occurs within the nanoparticulate system. A successful wire-bonding process step has been achieved only on textured printed films since the mechanical properties are enhanced. Tailoring of sintering and interdiffusion by reducing nanoparticles size is a attractive candidate to lower the working temperature, thus allowing the process to be compatible with microelectronics packaging.

## ACKNOWLEDGMENTS

Authors would like to thank Mr. Thierry Malia for his precious support on this study. Presented printings were conducted on the JetPac equipment developed in the lab with funding from EU (ERDF) and local authorities' research initiatives.

This work was supported by funding from the ANRT association and the EURIPIDES office through COSY-3D project.

## REFERENCES

1. D. Kim and J. Moon, *Electrochem. Solid-State Lett.* **8**, J30 (2005).
2. P. Buffat and J.-P. Borel, *Phys. Rev. A* **13**, 2287 (1976).
3. Q. Jiang and F. G. Shi, *Journal of Material Science and Technology* **14**, 171 (1998).
4. M. A. Asoro, D. Kovar, Y. Shao-Horn, L. F. Allard, and P. J. Ferreira, *Nanotechnology* **21**, 025701 (2010).
5. C. L. Chang, Y. C. Chuang, and C. Y. Liu, *Electr. Solid-State Lett.* **10**, H344 (2007).
6. T.-H. Kao, J.-M. Song, I.-G. Chen, T.-Y. Dong, and W.-S. Hwang, *Nanotechnology* **18**, 435708 (2007).
7. A. F. Mayadas and M. Shatzkes, *Phys. Rev. B* **1**, 1382 (1970).
8. R. Cauchois, M. Saadaoui, J. Legeleux, T. Malia, B. Dubois-Bonvalot, K. Inal, and J.-C. Fidalgo, 3<sup>rd</sup> *IEEE Electronic System-Integration Technology Conference*, AP-4 (2010).
9. C. V. Thompson and R. Carel, *Materials Science and Engineering B* **32**, 211 (1995).
10. Q. Jiang, S. Zhang, and J. Li, *Solid State Communications* **130**, 581 (2004).