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# **A novel approach to minimize the number of controls in Defectivity area**

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## **I. Introduction**

The transition from 200-mm to 300-mm wafers has seen the introduction of numerous controls at different stages of manufacturing in the semiconductor industry. This is because increasing the size of the wafer combined with a reduction in the size of the transistor has made more expensive the price of a wafer [1].

In this study, we investigated the case of controls in the defectivity area for the CMP (Chemical Metal Polishing) workshop and proposed a solution and a prototype which helps to highlight when too many measurements are done for “nothing” and when there is a lack of measurement. The solution proposed here is based on real time data analysis and risk computation in terms of number of wafers processed on a production tool since the last control. This notion is called Wafer At Risk [2][3]. It helps to reduce the work in the defectivity area and reorganize some activities in the fabrication line of ST Microelectronics Crolles.

## **II. Description of the study**

The goal of this study is to master the risk of processing a lot on a tool using real time data analysis and to minimize the number of controls. It consists in sampling lots in order to minimize risks. To each lot is associated a risk array. This array contains the new value of each risk (or of the risk reduction) if the lot is measured. And when a lot is measured in the defectivity area, the risks of various tools are reduced [2] [3].

The evolution of the risks might be controlled by warning and inhibit limits. The question asked here was: how to be sure that the Inhibit limit would not be exceeded to avoid the case of lack of control and how to know and determine the right time for a measurement to avoid “unnecessary” control?

## **III. First results and conclusion**

The algorithm, based on the idea described in the paper, has been implemented and tested on real instances of the industry. The algorithm has been embedded in a prototype. After two weeks of utilization of the prototype, a first analysis helped to highlight the major case of over-control and lack of control.

## **IV. References**

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[3] M. Shanoun, M. Bassetto, S. Bastoini, P. Vialletelle (2010). **Optimization of the process control in a semiconductor company : model and case study of defectivity sampling.** *International Journal of Production Research*