

# A Novel Approach to Minimize the number of Controls in Defectivity Area (13th Technical Meeting of ARCSIS, Rousset 2010)

Justin Nduhura Munga, Claude Yugma, Stéphane Dauzère-Pérès, Philippe Vialletelle

## ▶ To cite this version:

Justin Nduhura Munga, Claude Yugma, Stéphane Dauzère-Pérès, Philippe Vialletelle. A Novel Approach to Minimize the number of Controls in Defectivity Area (13th Technical Meeting of ARCSIS, Rousset 2010). 2010. emse-00605651

## HAL Id: emse-00605651 https://hal-emse.ccsd.cnrs.fr/emse-00605651

Preprint submitted on 3 Jul 2011

**HAL** is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers. L'archive ouverte pluridisciplinaire **HAL**, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.

## A novel approach to minimize the number of controls in Defectivity area

Authors: J. Nduhura<sup>1, 2</sup>, C. Yugma<sup>1</sup>, S. Dauzère-Pérès<sup>1</sup>, P. Vialletelle<sup>2</sup>

#### I. Introduction

The transition from 200-mm to 300-mm wafers has seen the introduction of numerous controls at different stages of manufacturing in the semiconductor industry. This is because increasing the size of the wafer combined with a reduction in the size of the transistor has made more expensive the price of a wafer [1].

In this study, we investigated the case of controls in the defectivity area for the CMP (Chemical Metal Polishing) workshop and proposed a solution and a prototype which helps to highlight when too measurements are done for "nothing" and when there is a lack of measurement. The solution proposed here is based on real time data analysis and risk computation in terms of number of wafers processed on a production tool since the last control. This notion is called Wafer At Risk [2][3]. It helps to reduce the work in the defectivity area and reorganize some activities in the fabrication line of ST Microelectronics Crolles.

### II. Description of the study

The goal of this study is to master the risk of processing a lot on a tool using real time data analysis and to minimize the number of controls. It consists in sampling lots in order to minimize risks. To each lot is associated a risk array. This array contains the new value of each risk (or of the risk reduction) if the lot is measured. And when a lot is measured in the defectivity area, the risks of various tools are reduced [2] [3].

The evolution of the risks might be controlled by warning and inhibit limits. The question asked here was: how to be sure that the Inhibit limit would not be exceeded to avoid the case of lack of control and how to know and determine the right time for a measurement to avoid "unnecessary" control?

#### III. First results and conclusion

The algorithm, based on the idea described in the paper, has been implemented and tested on real instances of the industry. The algorithm has been embedded in a prototype. After two weeks of utilization of the prototype, a first analysis helped to highlight the major case of over-control and lack of control.

#### **IV.** References

[1] A-J Su, J-C Jeng, H-P Huang, C-C Yu, S-Yu Hung, C-K Chao (2007). Control relevant issues in semiconductor manufacturing: overview with some new results. Control Engineering Practice 15 (2007) 1268-1279

[2] S. Dauzere-Pérès, J-L Rouveyrol, C. Yugma, P. Vialletelle (2010). A smart sampling algorithm to minimize risk dynamically. [Accepted in Advanced Semiconductor Manufacturing Conference, San-Francisco, USA, San Francisco, July 2010]

[3] M. Shanoun, M. Bassetto, S. Bastoini, P. Vialletelle (2010). **Optimization of the process control in a semiconductor company: model and case study of defectivity sampling**. *International Journal of Production Research* 

<sup>&</sup>lt;sup>1</sup> Ecole Nationale des Mines de Saint-Étienne - Centre Microélectronique de Provence - Site Georges Charpak, 880 Avenue de Mimet, F-13541 Gardanne France

<sup>&</sup>lt;sup>2</sup> STMicroelectronics, 850 Rue Jean Monnet, 38920 Crolles