Chip integration using inkjet-printed silver conductive tracks reinforced by electroless plating for flexible board packages

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Abstract

Inkjet-printing of interconnects is a maskless technology that has attracted great interest for printed electronics and packaging applications. Gemalto is expecting by motivated and developing skills and knowledge in this area to be at the forefront of European Security innovation and to answer to a continuous market pressure for higher security, lower cost and more secure complex systems. With an increasing need for flexible and mass deliveries of advanced secure personal devices such as: electronic passports, ID cards, driver licenses, other smartcards, e-documents and tokens. EMSE is seeing in these new developments an exciting brand new area of research situated between material science and electronics. In this frame, deposit and pattern creation for chip interconnection require specific behaviors which have to be scientifically understood to pursue industrial harmonious implementation.
Both groups collaborated on inkjet-printed electronic routing from deposition to sintering and characterization, using collaborative means provided on Micro-PackS platform.

Key words: Inkjet-printing, flexible electronics, chip interconnection, electroless, conductive nanoparticles, routing.

I-Introduction

The inkjet-printing technique of conductive nanoparticles, immediately followed by a sintering step, allows the reduction of process steps by a factor of three compared with common photolithography. The later is basically divided in six steps consisting in coating the base layer with several materials, before masking to transfer the circuitry patterns from a dedicated mask. After that, etching and stripping steps are performed. On comparison, the inkjet process is limited to the pattern direct-printing on the base layer and to the curing of the deposited ink in order to remove solvents, to initiate the film cohesion and to improve electrical contact between nanoparticles [1-3]. This additive approach is thus time and cost-saving for the fabrication of 2D interconnects and passive electronics. Nonetheless, films produced by this technique are usually nanoporous which simultaneously affects the electrical and the mechanical properties of printed structures [4,5].

In this paper, we describe how inkjet printing technology can suitably be used for IC chip integration through a direct writing approach. Direct flip chip on conductive tracks, routing on embedded chip and wire bonding are notably addressed. Each possibility is discussed in term of process steps. The inkjet technique is detailed and we report new developments of wire-bondable pads for flexible chip-on-board and lead-frame applications using thin films made of sintered silver nanoparticles followed by nickel electroless plating. In fact, low electrical resistivity of nanoporous silver is obtained through the optimization of sintering temperature ramps. Mechanical characterization shows that the Young's modulus and hardness still has to be improved for gold wire bonding process. This is achieved by surface finishing using nickel plating that shows a dependency to the initial microstructure of printed silver pads especially by affecting adhesion strength at the silver/nickel interface. The present technology is demonstrated through the implementation of IC chips in flexible boards

II-Type of chip integration using inkjet.

Printed electronics is particularly attractive for industrials looking for new integration form factors, and more specifically with the perspective to obtain thin and even flexible devices. Indeed, printed electronics broaden the number of possible applications which opens ways towards thin and flexible devices. In the short term, the active part of will remain Si based in most applications. Only some passives and electrical routing may be carried out using printed electronic means as inkjet. Consequently the first step in this kind of new integration is to properly interconnect the chip to the flexible substrate. In the Figure 1 are represented three possible chip interconnections to an electrical routing. In Figure 1.a, the chip is wire-connected using Au or Al wire-bonding to the beforehand printed Ag routing. While very simple, this prototyping process flow doesn't lead to very thin devices. Indeed, the chip and wires has to be subsequently protected with a glob top before further steps. This case is more extensively developed in the paragraph IV with a reliable solution on re-enforced path. In Figure 1.b, as in the previous solution, the routing is created first (printing and sintering) before transferring the silicon die with a flip chip process. This manufacturing process requires the deposition of conductive bumps on the original Al pads to enable the electrical interconnection with the electrical routing. An underfill glue, such as ACP, is required to maintain the mechanical contact. Positioning of the chip on the conductive tracks has to be performed accurately and carefully, regarding the thickness of the Ag NP layer (less than 1 µm). The applied force is related as much to the number of bumps to interconnect, than to the underlying substrate. This solution looks very compact and drives to flexible modules (see Figure 2). The thickness of the chip (thinner is better regarding the flexibility) and its size are to be particularly considered regarding the CTE mismatch issues arising from the heterogeneous multimaterial assembly that can eventually lead to a discontinuous electrical contact. In Figure 1.c, a more original and advanced chip integration version is depicted. A chip with a Ni-Au finishing on pads is embedded in the substrate. It could be done using molding or under vacuum lamination. The Ag-NP routing is subsequently performed both on the substrate surface and on the chip in a single pass. The inkjet-printing technology is particularly suitable for this kind of integration process. In particular, the electrical routing can easily be recalculated by software, if need be, after the molding step where an an unwanted and uncontrolled IC flowing can occur. This discrepancy cannot be corrected with a conventional lithography process. This solution should drive to very thin modules but, the inkjet-printed electrical pattern being performed directly after the molding step, the yield of inkjet technology should be sufficiently high to limit the discard rate of devices.

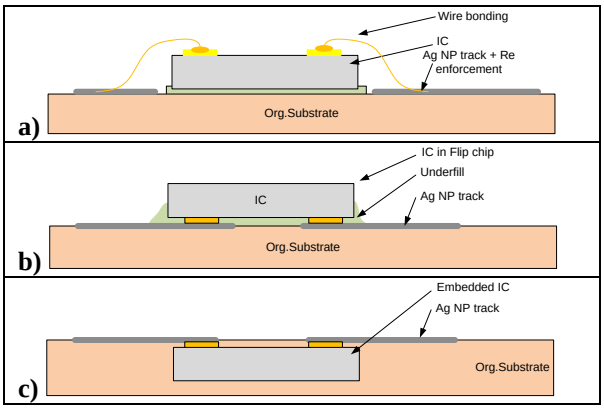

Figure 1: Type of possible chip integration: a) Standard wire bonding, b) Flip chip, c) Chip embedding .

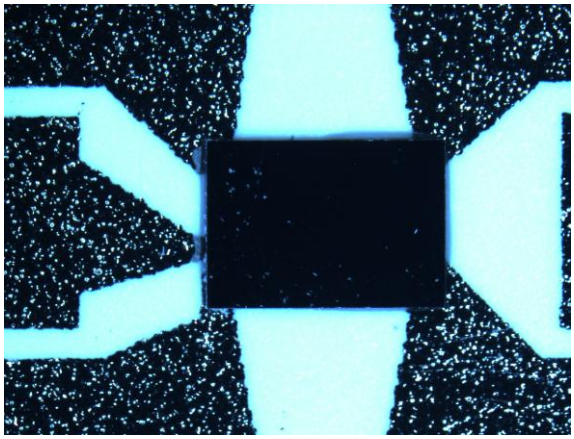

Figure 2: IC interconnected by flip chip to Ag NP tracks on PET substrate.

III-Ink-jet silver nanoparticles tracks.

Tuning of inkjet printing parameters

Patterns have been designed and printed using 40 nm silver nanoparticles ink on A4 Kapton sheet. Test structures include Kelvins, wire-bonding chain pads, a lead-frame for IC chips rerouting and squares for Young's modulus measurements and pull-off adhesion characterization (figure 3). An in-line inkjet printer prototype developed in the lab (JetPac) was employed to pattern the test vehicle. This fully automated prototype allows sequential pre-treatment and post-processing of printed substrate. The inkjet system is based on drop-on-demand technique which operates by propelling 30 pL droplets through each of the 256 nozzles. Ejections are driven by a bipolar pulse waveform sent to a piezoelectric print head which control the volume and the ejection velocity of droplets. An automaton ensures the coordination between the conveyor speed and the piezoelectric operating frequency for achieving patterns with line width inferior to 100 µm. A commercially available 125

µm thick Kapton HN polyimide substrate from DuPont has been selected for its flexibility, chemical resistance and low shrinkage behavior at curing temperature up to 350°C.

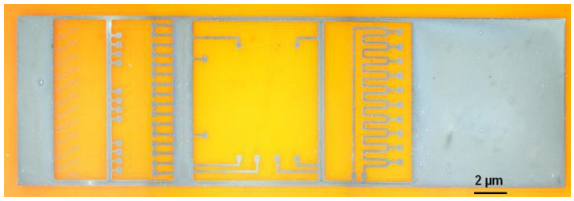

Figure 3: Inkjet-printed test structures on Kapton substrate.

Microstructural evolution with sintering.

Once silver lines are properly printed on the substrate, their electrical conduction is activated by the evaporation of solvents and by the sintering of metallic nanoparticles. Both of these steps are activated by thermal energy. The sintering step is achieved by providing thermal energy to nanoparticles in order to initiate diffusion regimes that will consequently cast bonds between nanoparticles. This phenomenon, called the Gibbs-Thomson effect, results from significant contributions of the surface energy to the free energy of the system. Due to their high value of surface area to volume ratio, diffusion regimes in silver nanoparticles are activated at lower temperature than the bulk melting point (961°C) [6,7].

The electrical properties of the printed thin-film are closely linked to the time and temperature couple during sintering. Since the mean free path of electrons in silver (λ=53nm) is of the same order of the nanoparticles average radius (<r_0>=40nm), electrical resistance between nanoparticles is a combination of ohmic and ballistic transport [8]. In the table 1 is reported for different temperature ramp the resistivity variation function of the grain diameter. Two times silver resistivity bulk is obtained for the strongest ramp.

Table 1: Microstructural and electrical evolution of printed silver nanoparticles under different thermal ramping (200°C, 15min)

	0.1°C/s	10°C/s	50°C/s
Resistivity (µOhm-cm)	5.01	4.52	3.77
Mean grain diameter (nm)	24	42	57

This curing step can be carried out using either a conventional oven or other selective techniques such as laser, microwave and joule heating [9-11].

IV-Case of electroless re-enforcement for wire bonding chip interconnection.

Interconnects reinforcement by electroless nickel plating

Nanoporous films usually exhibit different mechanical properties compared to the bulk, especially when the elastic modulus and hardness are considered [12]. Basically, those two parameters have low values that are greatly affected by the porosity as well as by the grain size. For successful wire-bonding operation, a thick and harder pad metallization is required in order to absorb the stress resulting from wire loading.

The direct bondability of gold wire on printed silver pads has been performed by connecting the lead-frame to the IC chip. It has been observed that whatever the microstructure of silver, the bonding step failed. Pad damages including silver splash and lifting are observed showing that both cohesive and adhesive fracture modes occurred. Those failure observations were attributed to the low Young's modulus and hardness of sintered silver pads, compared to the gold mechanical properties.

This key issue has been addressed using selective electroless nickel plating for pads reinforcement for gold wire bonding. This process has been widely adopted in microelectronics industry for the past few years as a consequence to lead-free solders specifications and for under-pads damage protection. Electroless nickel is an auto-catalytic process that is deposited from a hypophosphated nickel bath. The growth of electroless nickel has been performed during 5 min in order to achieve a 1.7 µm-thick nickel layer. This thickness is sufficient to improve the wear mechanical resistance and the film hardness and tends to clog the film porosities (Figure 4).

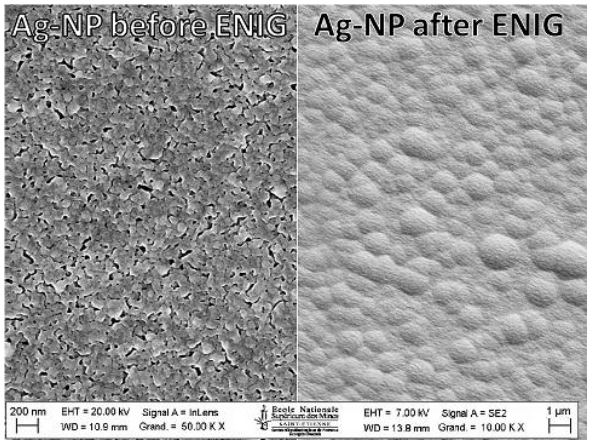

Figure 4: Layers of Ag NP after sintering (left) and after Ni-Au electroless growth (Right)

Ni-Au plating enabled wedge-bonding of 25µm diameter gold wire with a bonding force comprised between 18 and 20 g (See figure 5).

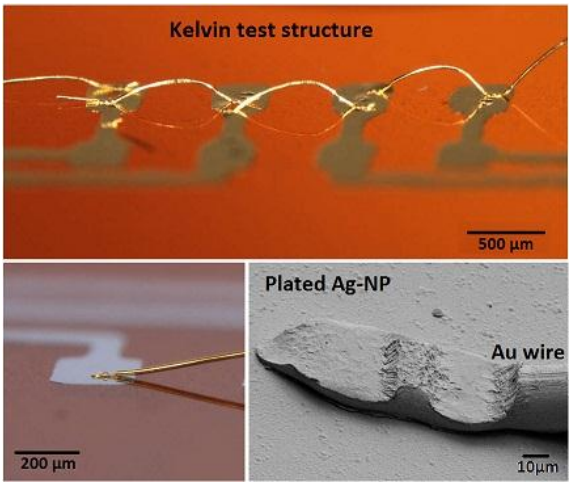

Figure 5: Gold wire-bonds on silver printed structures plated with electroless nickel process on a polyimide substrate.

Packaging performance

Once the feasibility is demonstrated, the process has to be validated by proving its capability in microelectronics systems. A flexible lead frame has thus been purposely designed and inkjet-printed on a polyimide substrate to host an IC chip in order to test performance of package from adhesion of plated interconnects to wire-bonds robustness, including contact resistance measurements between plated pads and gold wire. The testing package is shown on Figure 6.

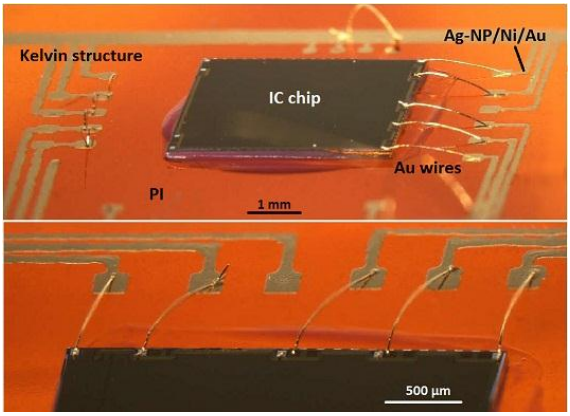

Figure 6: Dummy flexible package with wire-bonds from an IC chip to plated lead frame (front right and bottom) and between plated pads (front left).

The final validation came from the functionality test of the assembly where the IC-chip interconnected to the printed lead-frame using the above-mentioned technology has been reported in a ceramic package. The reporting step has been performed to be compatible with conventional electrical testing for microelectronic devices. Smartcard ISO pads on a PCB permitted Answer to Request query of the device, a test which happened to be conclusive with full functionality. This final test validated the pertinence of using inkjet printing jointly with electroless plating finishing for packaging applications.

V-Conclusion

In this paper, is exposed feasible IC integration where the electrical routing of the packaging may be performed using inkjet-printing. Flip chip and chip embedding drive to very compact package but some process steps must be well tuned. In the case of wire bonding interconnection we reported the latest developments. Wedge bonding of 25 µm diameter gold wire has been performed on finished surfaces using electroless nickel immersion gold plating process. The challenge, here, was to successfully perform wired connections on printed and malleable bond-pads whose thickness can fall down to 300 nm. The improved mechanical behavior has been correlated to the good performances of the wedge bonding. A functionality test finished to validate the process exposed in this paper for chip-on-flexible devices.

Acknowledgments

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