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Abstract

This paper shows that the well-know chalcogenide $Ge_2Sb_2Te_5$ (GST) in its amorphous state may be advantageously used as solid electrolyte material to fabricate Conductive-Bridge Random Access Memory (CBRAM) devices. GST layer was sputtered on preliminary inkjet-printed silver lines acting as active electrode on either silicon or plastic substrates. Whatever the substrate, the resistance switching is unambiguously attested at a nanoscale by means of conductive-atomic force microscopy (C-AFM) using a Pt-Ir coated tip on the GST surface acting as a passive electrode. The resistance change is correlated to the appearance or disappearance of concomitant hillocks and current spots at the surface of the GST layer. This feature is attributed to the formation/dissolution of a silver-rich protrusion beneath the AFM tip during set/reset operation. Beside, this paper constitutes a step toward the elaboration of crossbar memory arrays on flexible substrates since CBRAM operations were demonstrated on W/GST/Ag crossbar memory cells obtained from an heterogeneous fabrication process combining physical deposition and inkjet-printing.

1. Introduction

Resistive Random Access Memories (RRAM) are attracting intensive and increasing research efforts as potential high-density information storage solutions beyond the 15 nm node. [1,3] Various physical phenomena are known to lead to a non-volatile resistive switching effect which are related to different types of RRAM such as Thermo Chemical Memories (TCM) or Valency Change Memories (VCM). [4] The actual driving force for the resistance switching, although electrically induced in all cases, is quite different and depends upon the underlying resistive material. Among the main types of RRAM devices, Electro-Chemical Metallization memory cells (ECM), also referred as Conductive-Bridge Random Access Memories (CBRAM) or Programmable Metallization Cells (PMC)

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[5], are of particular interest due to their low-voltage operations [6,7], their large retention capabilities for more than 10-years [7] and their endurance larger than 10^5 cycles. [8,9] The memory elements simply rely on a solid electrolyte sandwiched between an electrochemically active metallic electrode (*i.e.* Cu or Ag) and an inert counter-electrode (such as Pt or W). The memory effect is achieved through redox mechanisms enabling the electro-migration of dissolved positives ions (*e.g.* Ag^+ or Cu^+) leading to an electro-deposition (set operation) or dissolution (reset operation) of metallic filaments between the two electrodes. Most of the solid electrolyte materials consist in a chalcogenide glass such as GeSe [7], GeS [10], Cu_2S [11] or oxide glasses such as SiO_2 [12] or Ta_2O_5.[13] An extensive summary of the electrolyte/electrode couples employed in CBRAM devices can be found in the recent work published by Valov *et al.* [5]. Although some works recommended the use of $Ge_2Sb_2Te_5$ (GST) layers as a way to improve the electrical behavior of CBRAM devices in terms of power consumption [14], resistance ratio (R_{OFF}/R_{ON}) [15] or electrical variability [16], few reports mention its use as a solid electrolyte. In previous works Pandian *et al.* [17]-[19] showed that crystallized Sb-rich GST layers exhibit Polarity Dependent Resistance (PDR) switching which was attributed to the formation/dissolution of Sb conductive filaments bridging together $Ge_2Sb_2Te_5$ crystalline grains and both electrodes through the amorphous GST phase. In complement to previously published works, the present paper demonstrates that amorphous $Ge_2Sb_2Te_5$ layer can also be used as a solid electrolyte in CBRAM devices employing silver as the active electrode. Using an heterogeneous fabrication process combining printed and/or sputtered electrodes and sputtered GST layer, CBRAM memory effect is clearly evidenced in the GST layer either at a nanoscale by conductive atomic force microscopy (C-AFM) or at a micrometric scale on crossbar cells with a W top electrode. In addition, in a context of constant development of new applications lying beside the silicon solid-state devices, memory material stacks were deposited on a flexible plastic substrate in view of future low-voltage embedded applications such as RFID (Radiofrequency Identification) systems.

2. Experimental details

Figure 1 illustrates the main fabrication steps of the samples. The substrates consisted in either Si(100) wafers covered by a 200 nm-thick SiO_2 layer or 120 µm-thick polyimide (Kapton® 500-HN) foils. At first, silver lines (350nm-thick, 100 µm wide) were deposited by inkjet printing of a commercial silver ink (SunChemical EDM5603) consisting of Ag nanoparticles with a diameter of about 80 nm in a mixture mainly composed of ethanediol and ethanol. The used printing head is a Spectra Galaxy JA 256/30 AA, providing ink drops of 30 pL. A printing resolution of 608 dpi was used. The patterns were printed at 300 mm/sec [Fig. 1(a)]. The samples were then annealed during 30 min at 200 °C in order to eliminate the organic solvent and favor the coalescence of the silver nanoparticles to produce conductive lines. The resulting silver lines were then covered by a GST thin film (thickness varying from 20 to 150 nm) deposited by radiofrequency (RF) magnetron sputtering from a high-purity (99.9999%) stoichiometric $Ge_2Sb_2Te_5$ target through a shadow mask [Fig. 1(b)]. Some of the samples were finally covered by an inert counter top electrode, consisting of W lines (200 nm thick, 100 µm wide) deposited by RF-magnetron sputtering through a shadow mask

perpendicularly to silver lines to produce crossbar devices [Fig 1.(c)]. The amorphous state of the GST layer after deposition on SiO_2/Si substrates was attested by means of x-ray diffraction [20].

Figure 2(a) shows a picture of a sample taken after the GST deposition (fabrication stage of figure 1(b)). The sample was also characterized by scanning electron microscope (SEM) at the same fabrication stage. The SEM cross-section of Fig. 2(b) shows a 135 nm-thick GST layer deposited on Ag printed lines on a Kapton® foil. The micrograph clearly shows a rough interface between the silver lines and the GST layer due to an incomplete coalescence of the Ag nano-particles during post-printing annealing.

The resistance switching in the memory stack (*i.e.* GST/Ag) was deeply investigated at nanoscales by means of conductive atomic force microscopy (C-AFM) on samples without a top electrode. The measurements were conducted on a Veeco Dimension 3100 with a Nanoscope V controller and platinum-iridium (Pt-Ir) conductive tip enabling the measurement of the local electrical conductivity. Local current-voltage characteristics were measured by applying a voltage bias to the bottom electrode, the AFM tip being grounded. Figure 3(a) shows a 5 µm × 5 µm atomic force microscope (AFM) image obtained in contact mode on a 35 nm-thick GST layer using an insulating silicon nitride tip. The calculated root mean square roughness of this topography map was 14.2 nm which is very close to the one obtained directly on the silver bottom electrode (14.6 nm). This result, in conjunction to the very low roughness measured on the same GST layer deposited on SiO_2/Si substrates [20], suggests that the roughness of the GST layer originates from the underlying printed silver electrode. This was confirmed by the extraction of cross-section profiles obtained either on the GST layer [Fig. 3(b)] or on the silver electrode [Fig. 3(c)] which exhibited similar roughness profiles.

3. Results and discussion

3.1. Resistive switching at a nanoscale on GST/Ag/SiO_2/Si stack

Atomic Force Microscopy (AFM) and its derivative electrical techniques have demonstrated their usefulness in studying resistive switching effects at a nanoscale [21]-[23]. Using a conductive Pt-Ir coated tip, current spectroscopy measurements were performed by means of C-AFM on a 35 nm-thick GST layer deposited on Ag printed lines. In those experimental conditions, the conductive AFM tip acts as a top electrode. While applying voltage sweeps in a range between -1.0 V and +1.0 V to the bottom electrode, the conductive tip being grounded, a neat hysteresis cycle loop is observed on the current-voltage characteristics as shown in Figure 4 where the different steps of the switching process are marked from 1 to 6. More precisely, at a bias voltage of 0.25 V the current level flowing through the tip suddenly overpasses the saturation current of the C-AFM sensor (*i.e.* 1.2 µA) (loop parts 1→3), the sample reaching a low resistance state (LRS). During the reverse sweep the I-V characteristic exhibits an ohmic behavior (4→5) down to a voltage of -0.1 V. Below this voltage, an abrupt current drop is observed, the measured current going down to the detection limit of the sensor (5→6) indicating that the sample returned back to a high resistance state (HRS).

This hysteretic I-V characteristic was measured while positioning randomly the tip on the GST layer and was observed in a very reproducible way at different locations on the sample; holding the tip at a fixed position, more than 10 switching cycles could be repeatedly obtained at a scan rate of 1Hz while avoiding thermal drift effects (*i.e.* tip sliding out of the probed region). The shape of the hysteresis loop together with the low voltage operations may be attributed to a conductive-bridge resistive switching effect.[5] This corresponds well to the creation (set) or dissolution (reset) of a metallic conductive filament formed by the electro-deposition of silver-rich aggregates underneath the AFM tip which produces a conductive pathway within the GST layer acting as a solid electrolyte (see inset 3 of Fig. 4). The different stages of the switching characteristic may be detailed as follow:

- From (1→3): starting from the pristine reset state, the set process occurs if a sufficient positive bias voltage (typically 0.25 V) is applied to the active electrode. The overall set process involves (i) the anodic dissolution of Ag creating Ag^+ cations in the GST film, (ii) the electromigration of the Ag^+ cations within the GST layer, (iii) the reduction of Ag^+ to Ag on the vicinity of the inert electrode (*i.e.* conductive AFM tip in present experimental conditions). This process leads to the formation of metallic filaments that bridge both electrodes. At this step, the memory element is in a low resistance state.
- From (4→6): by decreasing the applied voltage, the memory element remains in low resistance state unless a sufficient voltage of opposite polarity is applied with a subsequent electro-dissolution of the metallic filaments that enable switching back the memory element in a high resistance state.

Such low-voltage set and reset operations demonstrated at nanoscale using a conductive AFM tip are very encouraging in terms of scalability of CBRAM technology beyond sub-15 nm technological nodes.

In order to get a deeper understanding on the switching mechanism, a resistive switching cycle was sequentially performed on the GST layer as shown in Figure 5. Simultaneous topography [Figs. 5(a)-(c)] and current images [Figs. 5(d)-(f)] were recorded on a 0.5 µm × 0.5 µm area while applying a 100 mV voltage on the silver bottom electrode. In its initial pristine state (*i.e.* after GST deposition) the explored region does not exhibit any noticeable conductive spot as shown on the current mapping in Fig. 5(d). Upon applying a voltage pulse of +1 V for 1 s in the center of the scanned area (see inset of Fig. 5), a set operation was successfully achieved as demonstrated by the current spot observed within the center of Fig. 5(e). Concomitantly, the corresponding topographic image unambiguously shows the formation of a protrusion underneath the AFM tip upon applying the voltage pulse [Fig. 5(b)]. Interestingly, these correlated structural and electrical modifications are reversible and the hillock could be removed upon the application of a voltage pulse of the opposite polarity, restoring the original topographic and conductance images [Fig. 5(c) and Fig. 5(f)], *i.e.* reset operation. Let us note that similar results were obtained at several locations on several samples, attesting the reproducibility of the resistance switching mechanism.

The topographic profiles were extracted across the central region of Figs. 5(a)-(c), and are reported in Fig. 6(a). As already stressed by comparing Figs. 5(a) and 5(c), Fig. 6(a) demonstrates that a complete recovery of the initial morphology is achieved upon the application of a negative bias voltage on the silver electrode. From several sequential switching cycles, the lateral size of the protrusion was measured to be around 100 nm. An average hillock height of 10 nm was extracted by subtracting the initial topographic profile from the one obtained after the set operation [Fig. 6(b)]. Accordingly with the local I-V resistive-switching characteristics, the appearance (*resp.* disappearance) of the hillock can be attributed to the creation (*resp.* dissolution) of a silver-rich aggregate underneath the AFM tip during the application of the voltage pulse. Indeed, since there is no blocking top electrode, silver atoms may diffuse out of the chalcogenide layer and then accumulate underneath the AFM tip during the reduction and growth process. Nayak *et al.* previously reported such an observation during scanning tunneling microscopy (STM) measurements on Ag_2S-based atomic switches.[24] The large lateral extension of the conductive protrusion with respect to the contact area between the tip and the sample surface (which can be estimated around few tens of nanometer-square [21]) can be related to the water meniscus formed around the AFM tip placed under atmospheric conditions. [25]. As already reported in a previous work [22], the water meniscus may also act as an electrolyte within which metallic ions may move toward the metallic tip to be electrochemically reduced. Therefore the total width (100 nm) of the electrodeposited protrusion results from interplay between the extension of the field lines generated underneath the AFM tip, which is in the order of the contact area [23], the complex contact between the apex of the tip and the surface roughness and the diameter of the water meniscus formed around the tip which can be, at first order, as large as 2 times the radius of curvature (r_C) of the tip (r_C~25 nm in our experiment), depending on atmospheric conditions.

3.2. Resistive switching at a micro-scale induced by nano-lithography

Since the AFM tip consists in a moving top electrode, it can be used to switch a wider area through the application of a negative tip bias (with respect to the grounded bottom electrode) while scanning the surface.[26] Fig. 7(a) shows the current map of a pristine 10 µm × 10 µm GST region obtained at a reading sample voltage (V_S) of +50 mV. The scanned area is initially in a high resistance state since no current spot is detected. By scanning concentric regions at a slow scan speed (0.1 µm/s) and using alternately positive and negative sample bias voltages of +1V/-0.5V [Fig. 7(b)], it was possible to selectively write (*i.e.* set) or erase (*i.e.* reset) square-shaped regions as shown on the C-AFM of Fig. 7(c) recorded using a reading sample voltage value (V_S= +50 mV). Continuous capture of C-AFM images with the same tip bias showed that the written (*i.e.* bright) regions of Fig. 7(c) persisted over a timescale of half an hour.

3.3. A step toward crossbar memory array on flexible substrate

In the same manner, GST/Ag stacks deposited on Kapton® foils were also studied by means of current spectroscopy performed by C-AFM as depicted in the inset of Fig. 8(a). As it can be seen, the shape and orientation of the I-V loop is the same that the one obtained in Fig. 4, this feature indicating that the resistive switching also originates from a conductive-bridge mechanism. Even though set and reset voltages are slightly smaller than those obtained on silicon substrate (*cf.* Fig. 4), the GST/Ag stack still exhibits an unambiguous memory effect on a plastic substrate. In complement, individual memory elements defined by the 100×100 μm^2 cross-point area between perpendicular Ag (bottom electrode) and W (top electrode) lines were also electrically characterized in ambient conditions using an HP4156C analyzer (Agilent Company). I-V curves were measured from staircase voltage sweeps applied to W top electrode, while the Ag bottom electrode was kept at the ground level. Set and reset operations were achieved upon applying sweeps 0 → +1.5 V → –1.5 V → 0 V. The corresponding I-V characteristic is shown on Fig. 8(b). It exhibits a similar memory effect than during C-AFM measurements. From the I-V curves of Fig. 8, the low resistance state value was estimated around 500 Ω for the crosspoint device, while a value of 50 kΩ was found in the case of the C-AFM experiment on GST/Ag. The 100 times ratio between both resistance values does not follow the area scaling factor between the active areas involved in the switching process which is in the range of 10^8 considering a 10×10 nm^2 tip-sample contact area. This result illustrates the weak area dependence arising from the filamentary conduction process in CBRAM devices where the current level in the low resistance state is controlled by the number of conductive filaments bridging the top and bottom electrodes rather than by the active area of the device [7]. Finally one can also notice the difference observed in set/reset voltage values between both experiments. In each case a smaller programming (*i.e.* set or reset) voltage value was obtained in the case of the C-AFM measurements. Although this latter observation needs further clarification, one can invoke the electric field enhancement effect produced in the vicinity of the AFM tip [27] which may improve the migration of metallic ions during set or reset process. In addition, since set and reset processes are electrode-dominated in the case of conductive-bridge devices [5], the difference in set/reset voltages may also originates from the different electronic properties, such as work function of the electrode material, where the ~800 mV difference observed between set voltages almost corresponds to the work function difference between W (4.55 eV) [28] and platinum-iridium (5.3 eV).[29]

To summarize, these above-mentioned results demonstrate the feasibility of crossbar CBRAM memory elements fabricated on a flexible substrate by using heterogeneous elaboration processes combining conventional physical thin film deposition and inkjet-printing. Future measurements, including retention, cycling and robustness against mechanical stress (*e.g.* bending, stretching…) will be performed in order to assess the performances of such memory cells for future electronic applications on flexible substrates.

4. Conclusions

In summary, this paper demonstrates that amorphous GST thin film may act as a suitable solid electrolyte for conductive-bridge memory devices on flexible substrate. Memory elements were fabricated in combining inkjet-printed silver lines as active electrode and GST layer sputtered either on silicon or plastic substrates. Resistance switching was unambiguously demonstrated at a nanoscale from conductive-AFM measurements using a Pt-Ir coated tip as an inert counter-electrode. Sequential set/reset operations achieved during C-AFM measurements revealed that the resistance switching is accompanied by the reversible formation of a conductive hillock underneath the AFM tip. Based on these results, resistance-switching mechanisms was interpreted in terms of electrodeposition/dissolution of silver-rich conductive filaments within the GST layer. This memory effect was also evidenced at a micrometric-scale by means of nano-lithography as well as on individual crossbar memory elements fabricated on plastic foil and featuring a tungsten top electrode. These promising results constitute a first building block toward the elaboration of conductive-bridge memories on flexible substrates.

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Figure Caption

Figure 1. Description of the main fabrication steps of the studied devices. **(a)** Silver electrodes were obtained from printing of silver ink on substrates consisting either in SiO_2(200 nm)/Si wafers or plastic foils. **(b)** A GST layer was then deposited by radiofrequency magnetron sputtering on top of the silver lines through a shadow mask. **(c)** Finally W lines were sputtered through a shadow mask to form crossbar memory structures.

Figure 2. (a) Picture of a sample obtained from a plastic substrate consisting of printed silver lines covered by a 135 nm GST layer. The total surface of the GST layer is about 1cm×1.5cm **(b)** Corresponding cross-section SEM view of the sample.

Figure 3. (a) 5µm×5µm AFM topographic image obtained on the GST layer. **(b)** Cross-section profile obtained on the GST layer and **(c)** on the silver electrode.

Figure 4. Typical current-voltage characteristic recorded during C-AFM I-V spectroscopy on a 35 nm thick GST layer sputtered on printed Ag lines electrode deposited on a SiO_2/Si substrate. Schemes referenced from 1 to 6 indicate the orientation of the hysteresis loop and the insets propose a description of the resistive switching phenomenon at its different stages.

Figure 5. (a)-(c) Topographic and corresponding **(d)-(f)** current images measured on the top of the GST layer. Each current map was recorded using a sample bias of 100 mV, the tip being grounded. **(a)** Initial topography and **(d)** current mappings. **(b)** and **(e)** show the morphological and local current modifications induced upon applying a voltage pulse of 1V for 1 s to the bottom electrode, the tip being located in the center of the scanned area. Upon the application of a pulse of reverse polarity, the memory stack turns back in its original configuration as shown in **(c)** and **(f)**. White arrows indicate the modified region underneath the AFM tip during the application of voltage pulses, as depicted in the insets of the figure.

Figure 6. (color online) **(a)** Topographic profiles extracted from Figs. 5(a)-(c) across the central region as indicated in the inset. Dotted line shows the initial profile obtained from Fig. 5(a). The two other curves were obtained after set (*i.e.* 1V, 1s) and reset (*i.e.* -1V, 1s) operations from Figs. 5(b) and 5(c). **(b)** Extracted height of the protrusion.

Figure 7. (a) Current map of a virgin GST/Ag stack measured at V_S=+50mV. **(b)** Scheme of alternately biased regions used to write or erase the memory stack. **(c)** Resulting current map measured at V_S=+50mV.

Figure 8. I-V characteristics measured on a GST/Ag/Kapton® stack **(a)** at nanoscales by C-AFM or **(b)** at a micrometric scale on a standard probe station. In this latter case, W top electrode was sputtered perpendicularly to Ag lines to form a crossbar structure.

FIGURE 1

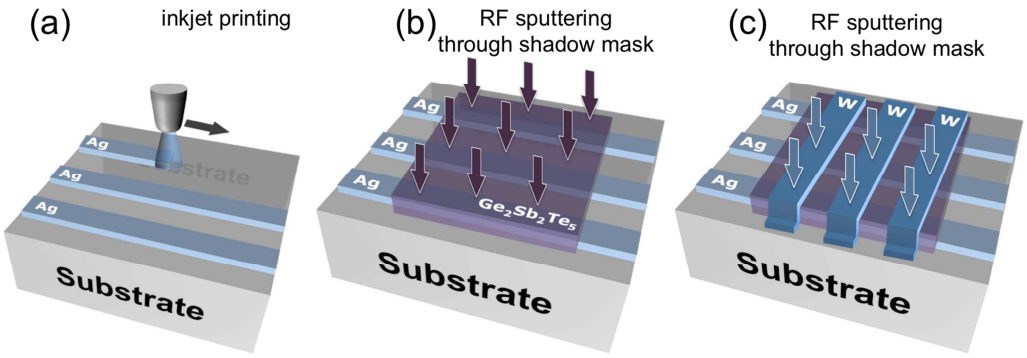

(a)
inkjet printing
Ag
Ag
Ag
Substrate
(b)
RF sputtering
through shadow mask
Ag
Ag
Ag
Ge2Sb2Te5
Substrate
(c)
RF sputtering
through shadow mask
Ag
Ag
Ag
W
W
W
Substrate

FIGURE 2

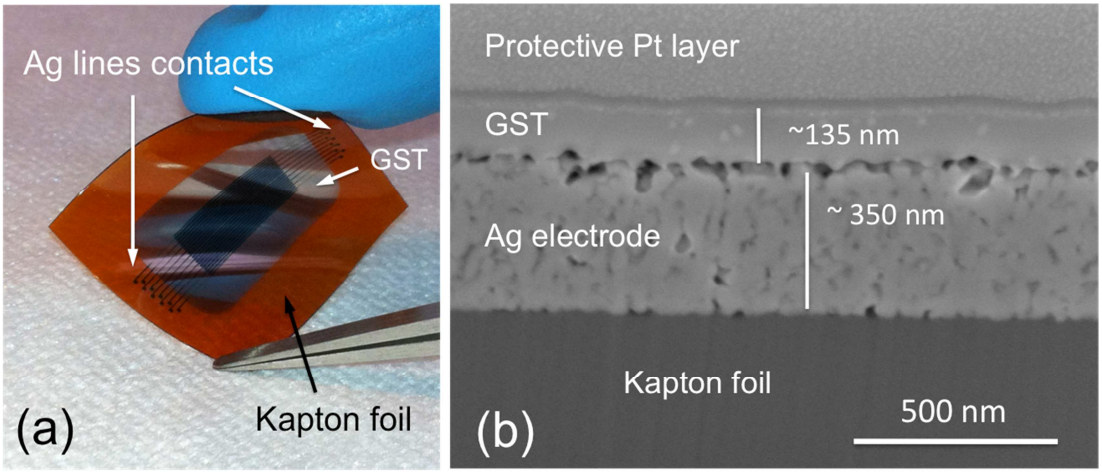

Ag lines contacts
GST
Kapton foil
(a)
Protective Pt layer
GST
~135 nm
~ 350 nm
Ag electrode
Kapton foil
500 nm
(b)

FIGURE 3

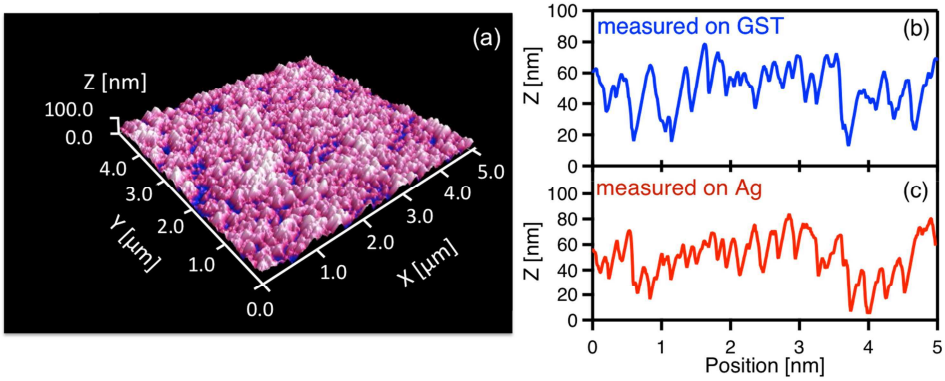

(a)
Z [nm]
100.0
0.0
4.0
3.0
2.0
1.0
0.0
Y [µm]
1.0
2.0
3.0
4.0
5.0
X [µm]
measured on GST
(b)
Z [nm]
100
80
60
40
20
0
measured on Ag
(c)
Z [nm]
100
80
60
40
20
0
0
1
2
3
4
5
Position [nm]

FIGURE 4

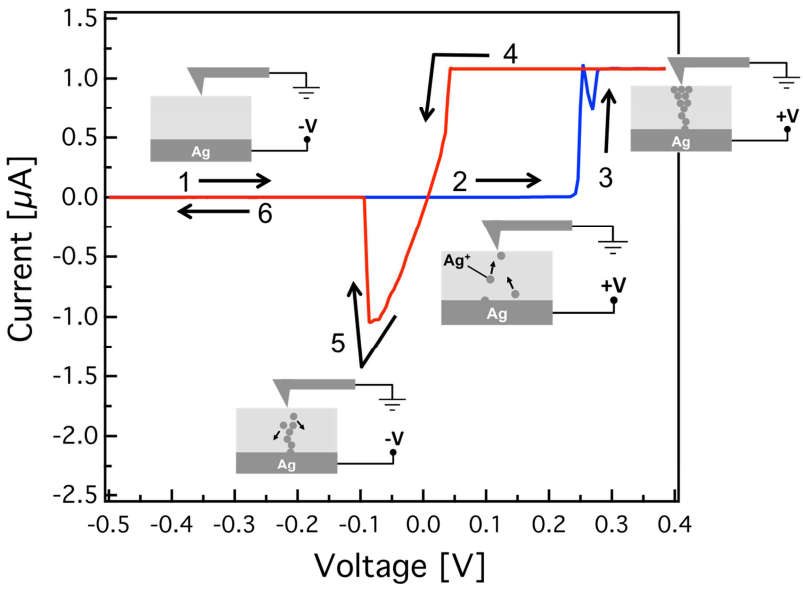

Current [μA]
Voltage [V]
1.5
1.0
0.5
0.0
-0.5
-1.0
-1.5
-2.0
-2.5
-0.5
-0.4
-0.3
-0.2
-0.1
0.0
0.1
0.2
0.3
0.4
1
2
3
4
5
6
Ag
-V
+V
Ag+

FIGURE 5

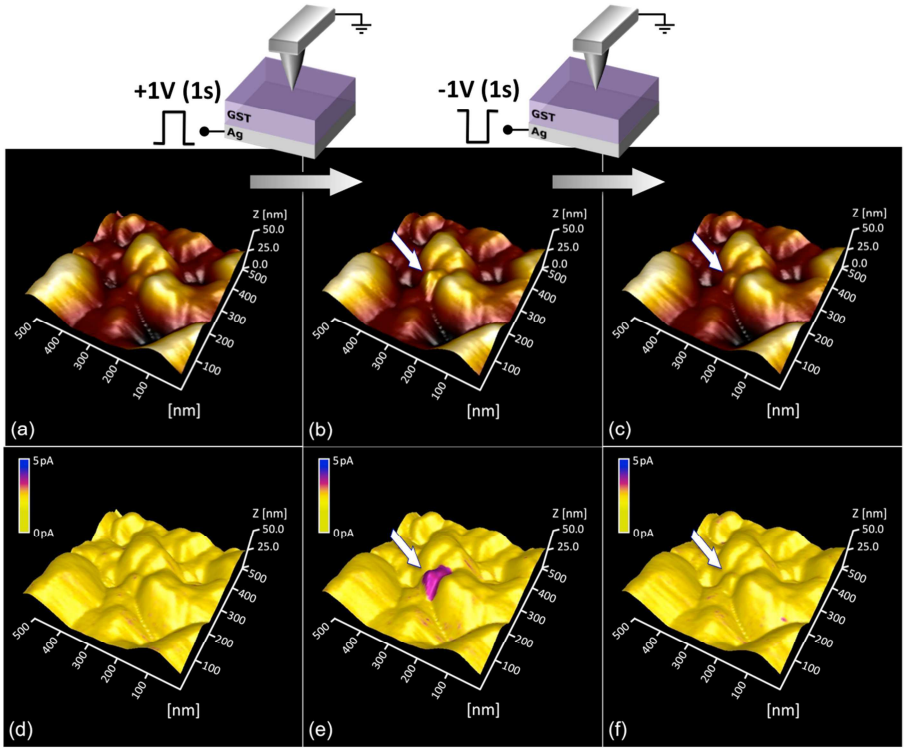


FIGURE 6

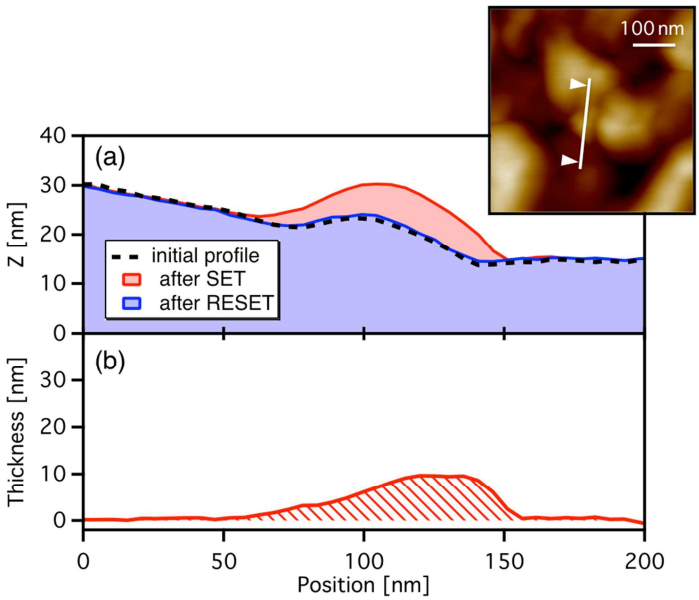

100 nm
(a)
Z [nm]
initial profile
after SET
after RESET
(b)
Thickness [nm]
Position [nm]
0
50
100
150
200
10
20
30
40

FIGURE 7

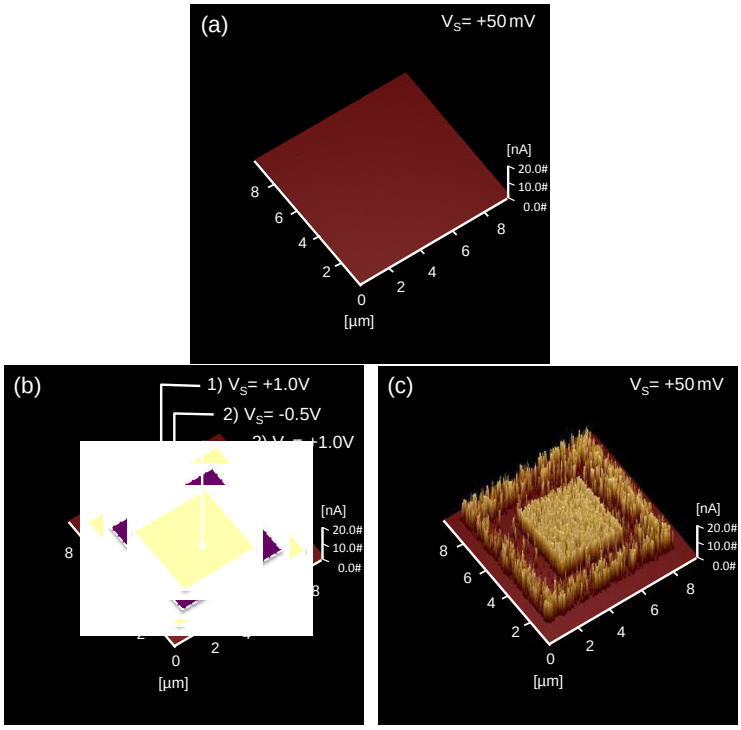
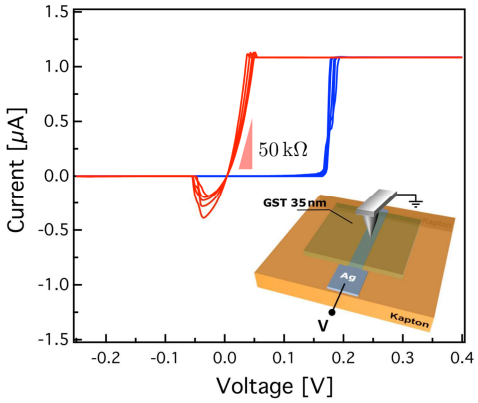
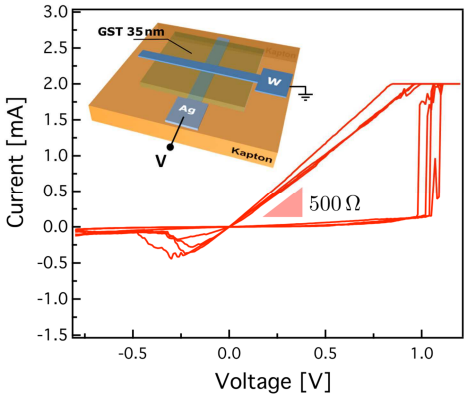

(a)
V_S= +50 mV
[nA]
20.0#
10.0#
0.0#
8
6
4
2
0
2
4
6
8
[µm]
(b)
1) V_S= +1.0V
2) V_S= -0.5V
[nA]
20.0#
10.0#
0.0#
8
0
2
[µm]
(c)
V_S= +50 mV
[nA]
20.0#
10.0#
0.0#
8
6
4
2
0
2
4
6
8
[µm]

FIGURE 8


Current [μA]
Voltage [V]
50 kΩ
GST 35 nm
Ag
Kapton
V

(a)


Current [mA]
Voltage [V]
GST 35 nm
W
Ag
Kapton
V
500 Ω

(b)