Improving the ability of Bulk Built-In Current Sensors to detect Single Event Effects by using triple-well CMOS

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Abstract

Bulk Built-In Current Sensors (BBICSs) were introduced to detect the anomalous transient currents induced in the bulk of integrated circuits when hit by ionizing particles. To date, the experimental testing of only one BBICS architecture was reported in the scientific bibliography. It reports an unexpected weakness in its ability to monitor NMOS transistors. Based on experimental measures, we propose an explanation of this weakness and also the use of triple-well CMOS to offset it. Further, we introduce a new BBICS architecture well suited for triple-well that offers high detection sensitivity and low area overhead.

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1. Introduction

Bulk Built-In Current Sensors (BBICSs) [1] were introduced to monitor the currents induced in the bulk of integrated circuits (ICs) by ionizing particle hits. Such currents may create transient errors into the circuit's calculations. BBICSs are used to detect unusual bulk currents and to possibly trig recovery mechanisms to maintain the circuit's functionality. This paper is organized as follows: Section 2 describes the principles underlying BBICSs. It also introduces the architecture of the only BBICS that was, to date, experimentally tested. Its weaknesses, revealed during the testing of the test chip, are discussed. These weaknesses are explained in section 3, on the basis of measurements of the bulk currents induced by a laser into the PN junctions found in CMOS circuits. In section 4, we propose the use of triple-well CMOS to obtain an improved detection capability. A new BBICS design well suited for triple-well CMOS is also introduced. Then, section 5 draws a conclusion.

2. State-of-the-art

ICs are known to suffer from Single Event Effects (SEEs) caused by ionizing particles in radioactive environments. In the following subsections we review the electrical phenomenon underlying SEEs and the principles of their detection by using BBICS. We also describe the architecture of the NMOS-BBICS designed by Zhang et al. [2] and the weakness revealed during its experimental testing with a laser [3].

2.1. Single Event Effects and related detection through bulk-current monitoring

When an ionic particle passes through silicon it generates electron-hole pairs along its path. These electrical charges generally recombine without any significant effect. However, the electron-hole pairs may be separated by the electric field found in a PN junction, thus creating a transient current. This phenomenon is generally introduced by studying the inverter case, see Fig. 1 as an illustration when the inverter's input is low (i.e. in = 0 and out = 1). In this configuration, the SEE sensitive part is the drain of the NMOS transistor, which is in OFF state (note that the PMOS drain is the sensitive part when the input is high: the sensitive part location is data dependent). The generated transient current, depicted by a current source in Fig. 1, flows through the PN junction existing between the N-type drain of the NMOS and the P-type substrate which is grounded. This current has two components: one passing through the PMOS transistor (in ON state), another discharging the output capacitance of the inverter (pictured in dotted lines). As a result of the latter, the inverter's output undergoes a transient alteration from 1 to 0. This voltage transient, also known as SET (or single event transient), may thus propagate through the circuit logic creating soft errors. Furthermore, whether a SET is induced directly in a memory element, the stored data may be flipped characterizing the so-called SEU (or single event upset, i.e. a soft error).

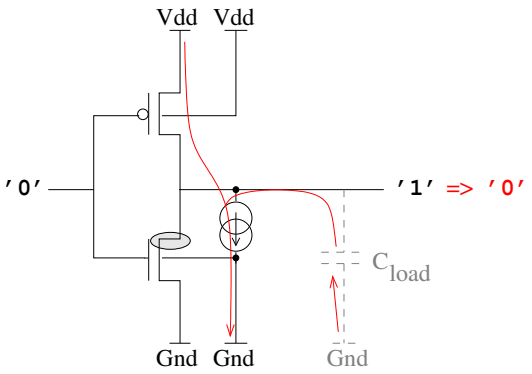

Figure 1: Single event transient mechanism: the inverter case.

A significant property of the transient current induced by an ionic particle is that it flows through the bulk of the struck sensitive transistor. BBICSs are designed to take advantage of this property: they monitor these bulk currents, hence they are able to detect unusual currents and, consequently, the advent of SEEs. Fig. 2 depicts the insertion of a BBICS between the bulk (the P-type substrate) of an NMOS transistor and the ground supply. The biasing of the P-substrate (node *NMOS_bulk*) is provided by the BBICS. Hence, as illustrated, any SEE induced current necessarily flows through the BBICS. The BBICS pur-

pose is then to raise a warning flag indicating that the circuit's function may be affected.

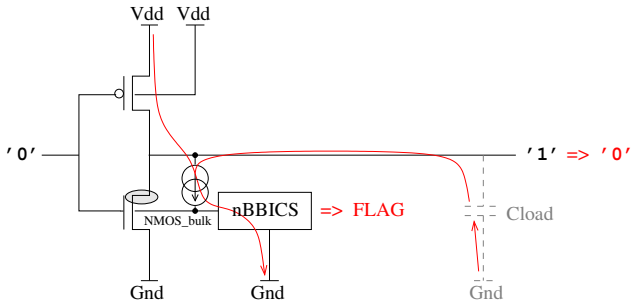

Figure 2: NMOS sensitivity monitoring with an nBBICS.

In Fig. 2, the BBICS used to monitor NMOS transistors is named a nBBICS. There also exists pBBICS dedicated to the monitoring of PMOS transistors. Even if pBBICS and nBBICS have different architectures they rely on the same principle, i.e. the monitoring of bulk currents.

2.2. *Zhang et al.* BBICS *architecture*

Among various BBICS architecture proposals [4, 5], only one [2] was experimentally tested [3]. The authors designed both NMOS- and PMOS-BVIS to monitor NMOS and PMOS. For the sake of brevity, we only report in Fig. 3 the architecture of their NMOS-BVIS (Built-In Voltage Sensor according to the authors' denomination).

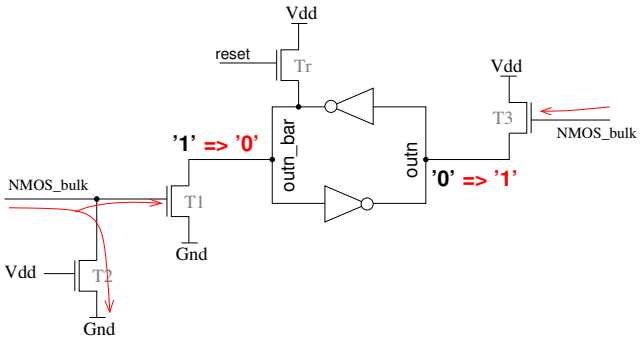

Figure 3: Architecture of the NMOS-BIVS.

The core part of this NMOS-BVIS is a memory latch made of two cross-coupled inverters. In normal operating conditions, node *outn* is at low level while node *outn_bar* is high. Node *outn* goes high to indicate the detection of any SEE induced bulk current. The BBICS connection to the P-substrate of the monitored transistors (node *NMOS_bulk* in Fig. 2) is used as a bias contact to Gnd through the ON transistors T2. When a particle hits a monitored sensitive area, the induced current (pictured in red) flows through the related PN junction into the input of the NMOS-BIVS: node *NMOS_bulk* in Fig. 3. A part of this current flows to ground through T2, another part charges the gate capacitances of transistors T1 and T3. As a result, node *NMOS_bulk*'s voltage rises, hence T1 and T3 pass from OFF to ON state making the core latch flip. Node *outn* goes high indicating an SEE current detection. As the transient current ceases, node *NMOS_bulk* returns to ground thanks to the always ON T2 transistor. Transistor Tr is used to reset the BBICS in its initial condition.

A key point in designing a BBICS is to obtain a detection threshold lower than the level of appearance of SEEs (the sensitivity threshold).

2.3. *Experimental testing of the* NMOS- *and* PMOS-BIVS

The NMOS- and PMOS-BVIS were tested experimentally, the test was performed on a test chip (CMOS 90nm) with a laser source to emulate the effect of an ionizing particle. The authors report the use of a one picosecond laser source at a $800nm$ wavelength [3]. The spot size was $1.6\mu m$ and the energy varied over a few hundreds pJ range. Their test chip embeds a multiplier as test element which is monitored by various NMOS- and PMOS-BIVS. The multiplier sensitivity threshold against laser illumination was found at a laser energy of 82pJ. The detection threshold of a BBICS increases with the number of standard cells it monitors. To evaluate this effect, different BIVS were connected to 10, 20, 40, 80, or 160 cells biasing contacts. Table 1 reports the obtained detection thresholds.

Table 1: Detection threshold of the NMOS- and PMOS-BIVS expressed as the minimal detected laser energy (pJ) given for various numbers of monitoring contacts (n.d. stands for 'not detected') extract from [3].

	Detection threshold (pJ)			
# of contacts	10	40	80	160
NMOS-BIVS	$110pJ$	$149pJ$	n.d.	n.d.
PMOS-BIVS	$15pJ$	$42pJ$	$75pJ$	n.d.

PMOS-BIVS detection threshold was found to be lower than the multiplier sensitivity threshold (82pJ) when monitoring up to 80 biasing contacts. However, even when monitoring only 10 biasing contacts, the NMOS-BIVS detection threshold (110pJ) was found higher than the multiplier sensitivity threshold (82pJ).

As a conclusion, NMOS-BIVS were found unable to detect all SEE occurrences on experimental basis. This result was unexpected because its relevance was previously ascertained on simulation basis [2, 3].

3. Analysis

3.1. Experimental measures

For the purpose of analyzing the weakness of the NMOS-BIVS, we performed a set of experiments on a test chip we designed to measure the currents involved in SEE generation. These measures were carried out on NMOS and PMOS transistors both for bulk and triple-well CMOS 90nm technology. We used an infrared laser source (1064nm) applied through the test chip backside to induce the transient currents. Current measurements and biasing of the test elements were done with probes. Due to measurement constraints, we used 20μs laser pulses at 1.25W with a spot size of 5μm. These laser settings are not consistent with the emulation of an ionizing particle strike. However, we were more interested in comparing the magnitude of the currents induced in the various PN junctions of transistors than in precisely emulating an SEE.

NMOS current: the sensitive part of an NMOS transistor is the Psub-N$^+$ junction of his drain when it is reverse biased. We measured a 2.5mA current flowing from the drain (biased at 1.2V) into the P-substrate biasing contact (grounded) as depicted in Fig. 4. The other electrodes of the transistor were left floating.

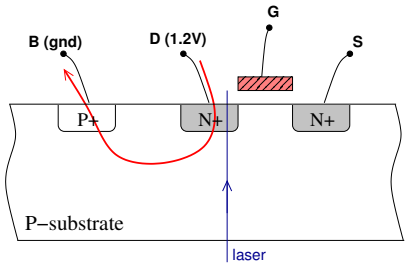

Figure 4: View of the laser induced current in the Psub-N$^+$ junction of an NMOS.

PMOS currents: the sensitive part of a PMOS transistor is the P$^+$-Nwell junction of his drain when it is reverse biased. The laser path to this junction also crosses the Psubstrate-Nwell junction (it is similar when hit by an ionizing particle). We performed a first measure letting unbiased the Psubstrate (see top part of Fig. 5). We measured a 1.9mA current flowing from the Nwell biasing contact (biased at 1.2V) into the drain (grounded). Then, we performed a second measure with the Psubstrate grounded, which is the proper biasing in normal operation of a chip (see bottom part of Fig. 5). We measured only a 200μA current flowing through the P$^+$-Nwell junction whereas we measured a 8mA current flowing through the Psubstrate-Nwell junction.

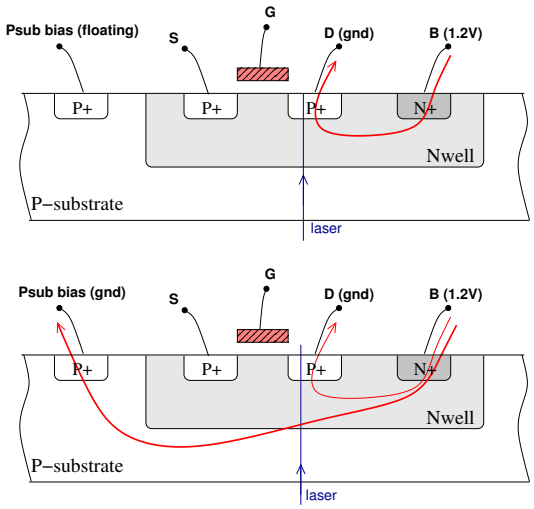

Figure 5: View of the laser induced currents in the P$^+$-Nwell and Psub-Nwell junctions of a PMOS: P-substrate unbiased (top), P-substrate grounded (bottom).

3.2. NMOS-BVIS weakness analysis

Current measurements on a PMOS showed that the induced current had two components: one of 8mA flowing through the Psubstrate-Nwell junction, one of 200μA flowing through the P$^+$-Nwell junction. SET are induced by the second one, while the first one may be monitored by a PMOS-BBICS. This explains why the PMOS-BVIS had a detection threshold lower than the multiplier sensitivity threshold: there is more than an order of magnitude between the two related current components.

This is different for a NMOS: there is only one current component flowing both through its sensitive drain and through its bulk biasing contact. Moreover, if an NMOS-BVIS is connected to this contact it will not collect the whole current because there are other current return paths to the ground on-chip (for the PMOS case the only current path is through the Nwell biasing contact). As a result, the weakness of the NMOS-BIVS has two causes: (a) it collects an SEE induced current lower than that collected by a PMOS-BIVS, and (b) the current it collects is lower than the current generating the SEE.

4. Improving BBICS efficiency

4.1. Use of triple-well CMOS

Modern CMOS technologies generally offer a triple-well option. It consists in embedding the NMOS transistors into P-type well (or Pwell) isolated from the Psubstrate. The Pwell containment is made laterally with Nwell implants and with a deep Nwell implant underneath. The deep Nwell and Nwell are electrically connected, both normally biased at 1.2V.

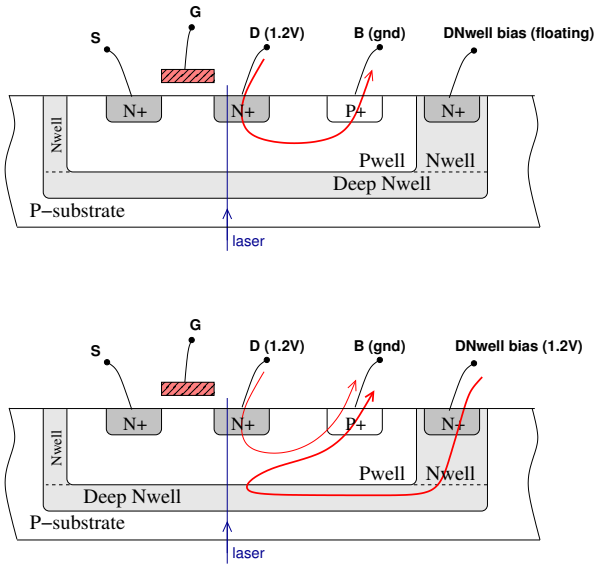

Figure 6: View of the laser induced currents in the Pwell-N$^+$ and Pwell-Nwell junctions of a triple-well NMOS: deep Nwell unbiased (top), deep Nwell biased at 1.2V (bottom).

Our assumption was that an NMOS in an isolated Pwell will have a similar behavior regarding the SEE currents as a PMOS. For validation purposes, we performed the same measurements on a triple-well NMOS as those done on bulk CMOS transistors (with the same laser settings as reported in 3.1). First we let the deep Nwell unbiased, second we biased it at 1.2V (see respectively the top and bottom parts of Fig. 6). With a floating deep Nwell, a 2.3mA current flowed through the NMOS drain Pwell-N$^+$ junction. With the deep Nwell biased at 1.2V, the NMOS drain junction current diminished to 200μA, whereas a 6mA current flowed through the Pwell-deep Nwell junction. These figures are similar to those of the PMOS. Using triple-well CMOS creates more than an order of magnitude difference between the lower current contributing to SEE generation and the higher current potentially monitored by a BBICS. On basis of these experiments we recommend the use of triple-well CMOS to obtain an optimal use of BBICS.

4.2. Single BBICS *architecture*

Description: we also developed a new BBICS architecture well suited for the monitoring of triple-well CMOS logic: the 'single BBICS' pictured in Fig. 7. It is designed to monitor simultaneously NMOS and PMOS (which are respectively enclosed in Pwells and Nwells): its *NMOS_bulk* and *PMOS_bulk* inputs are respectively connected to the Pwell and Nwell biasing contacts.

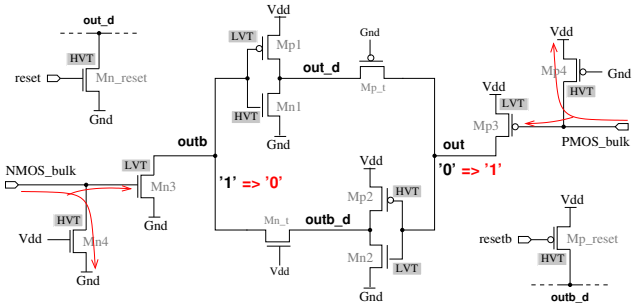

Figure 7: Architecture of the single BBICS.

The core part of the single BBICS is a latch made of two cross-coupled inverters. In monitoring state, node *out* is at low level while node *outb* is high. Node *out* goes high to indicate the detection of any SEE induced bulk current. The BBICS connection to the Pwell (resp. Nwell) of the monitored NMOS (resp. PMOS) (node *NMOS_bulk*, resp. node *PMOS_bulk*) is used as a bias contact to Gnd (resp. to Vdd) through the ON transistor Mn4 (resp. Mp4). When a particle hits a monitored sensitive area, the induced current (pictured in red) flows through the related PN junction into (resp. from) the corresponding input of the single BBICS. A part of this current charges (resp. discharges) the gate capacitance of transistor Mn3 (resp. Mp3): node *NMOS_bulk*'s (resp. *PMOS_bulk*'s) voltage rises (resp. decreases), hence Mn3 (resp. Mp3) passes from OFF to ON state, making the core latch flip. Node *out* goes high indicating an SEE detection. Transistors Mn_reset and Mp_reset are used to reset the BBICS in its monitoring state. Transistors Mn_t and Mp_t are used to ease the flipping of the core latch from the monitoring state to the alarm state. This flipping ability was also reinforced by using low and high voltage threshold transistors (denoted LVT and HVT in Fig. 7), as explained in [6].

This architecture brings together the NMOS and PMOS monitoring ability of NMOS-BVIS and PMOS-BIVS. Hence the area overhead is reduced from 16 transistors (8 + 8) to 14 transistors.

Validation on the basis of simulation: a test chip designed in a CMOS 65 nm process that embeds single BBICSs and various test structures is expected by the 2nd quarter of this year. We report in the following an evaluation, on the basis of simulation, of its very good efficiency to detect the advent of SEEs in triple-well CMOS. The electrical simulation results we report were conducted after parasitic resistances and capacitances extraction with a standard CAD tool (substrate resistances were not considered). For the

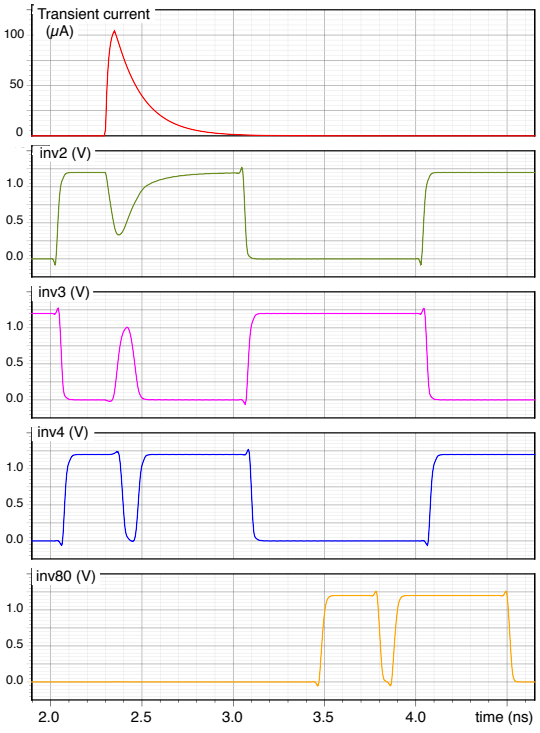

Figure 8: SET generation and propagation – 80 inverters chain, $104\mu A$ transient current magnitude (NMOS).

purpose of comparison, we first defined the SEE sensitivity threshold of the CMOS 65 nm process we used. We expressed it as the magnitude (in μA) of the SEE induced transient current pulse sufficient to give rise to the propagation of an SET along a chain of inverters. To obtain the lowest value of this sensitivity threshold, we used the smallest inverters among the standard cells. Note that the sensitivity threshold grows with the number of inverters. Fig. 8 reports the appearance of a SET caused by a transient current which magnitude is $104\mu A$. The timings ($\sim 50\,ps$ and $\sim 150\,ps$ rise and fall times, respectively) of the transient current we used in simulations are those reported in [7]. The transient current was simulated between the NMOS' drain of the 2nd inverter (node *inv2*) and the ground as illustrated in fig. 1. It propagated through the third and fourth inverters (nodes *inv3* and *inv4*) and the following ones to the output node *inv80*. Sensitivity thresholds obtained from simulation for transient current induced in NMOS or PMOS transistors and for various length of inverters chains are reported in table 2.

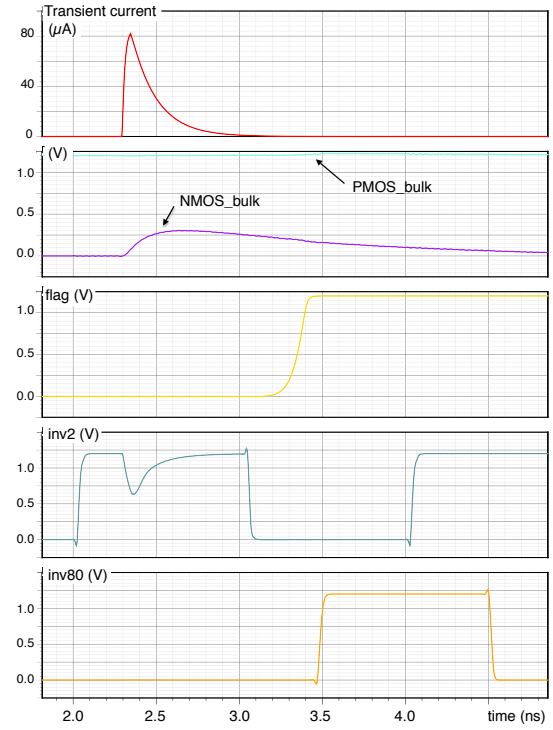

Figure 9: Single BBICS' alarm flag trigerring – 80 inverters chain, $82\mu A$ transient current magnitude (NMOS).

The next step was to obtain the detection threshold (i.e. the transient current magnitude sufficient to trigger an alarm) of the single BBICS when connected to the same chain of 80 inverters. The transient current magnitude was progressively decreased (the pulse timings were left unchanged) until reaching the least magnitude sufficient to trigger the alarm: $82\mu A$. Fig. 9 reports the signals of interest: the transient current, the voltage of nodes *NMOS_bulk* and *PMOS_bulk*, the flag signal, the outputs of the 2nd and 80th inverters. In response to the transient current, the flag went to high level indicating the advent of an SEE induced transient current. This current was too weak to induce an SET.

We ran simulations for both bulk and triple-well CMOS. The obtained results are given in table 2 (transient currents for both NMOS and PMOS SETs were simulated at the NMOS or PMOS drain of the 2^{nd} inverter of the chain). Regarding bulk CMOS, as suggested in section 3, for a chain of inverters length

above 120 inverters the sensitivity threshold for NMOS is lower than the detection threshold (underlined in bold in table 2): a SET may be induced without being detected. Whereas, the sensitivity threshold for PMOS remains higher than the detection threshold (we did not conducted simulations over 200 inverters): any SET would be detected.

Table 2: SET thresholds and single BBICS detection thresholds for bulk and triple-well CMOS as a function of the inverters chain length − SET NMOS/PMOS gives the sensitivity threshold (in μA) for a NMOS/PMOS transient current, BBICS detection gives the corresponding detection threshold (in μA) of the single BBICS.

SET and detection thresholds (μA), CMOS-bulk					
# of inverters	40	80	120	150	200
SET NMOS	102	104	**104**	**104**	**104**
BBICS detection	56	82	**107**	**125**	**155**
SET PMOS	126	131	134	135	137
BBICS detection	45	67	90	107	134

SET and detection thresholds (μA), triple-well					
# of inverters	40	80	120	150	200
SET NMOS	94	95	98	99	100
BBICS detection	75	112	147	173	212
SET PMOS	118	125	127	127	130
BBICS detection	84	125	163	191	237

Regarding triple-well CMOS, the results of table 2 should be considered with care to avoid minimizing its efficiency. Indeed, as illustrated respectively in the bottom parts of Fig. 5 and 6, the SEE induced currents flowing through the drain of the struck transistor is smaller than the total current flowing through the biasing contact of the transistor's well. Hence, the detection threshold is expressed as the transient current flowing through a Pwell or Nwell biasing contact, and the SET sensitivity threshold is expressed as the transient current flowing through the NMOS or PMOS drain. As a result, considering the NMOS SET sensitivity threshold for a 200 inverters long chain, the related $100\mu A$ current will only be a part of a much bigger current flowing through the NMOS' biasing contact into node *NMOS_bulk*: the latter will outpace the $212\,\mu A$ detection threshold.

Thus, the use of triple-well CMOS appears to solve the weakness of NMOS-BIVS [3] in detecting SEEs. Moreover, given the area of the single BBICS ($22.6\,\mu m^2$) and that of a sub-chain of 10 inverters in triple-well ($21.15\,\mu m^2$, $19.8\,\mu m^2$ for bulk CMOS), the area overhead for a 200 inverters chain is 5.4%.

5. Conclusion

Based on experiments, we explained the unexpected weakness of BBICS in monitoring SEE induced in NMOS transistors for bulk CMOS processes. Consequently, we suggest using triple-well CMOS to offset this weakness. Indeed, the enclosure of NMOS into isolated Pwells allowed BBICS to monitor an induced current that is an order of magnitude greater than the current contributing to the occurrence of an SEE. Moreover, the whole current will pass through the monitoring BBICS because there is no other return path to Gnd or Vdd. By using triple-well, the efficiency of NMOS-BBICS will be similar to that of PMOS-BBICS. Moreover, we introduced a new single BBICS architecture that brings together the NMOS and PMOS monitoring ability. It is well adapted to triple-well CMOS and reduces the area overhead.

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