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Abstract

This study is driven by the need to optimize failure analysis methodologies based on laser/silicon interactions inside an integrated circuit using a triple-well process. It is therefore mandatory to understand the behavior of elementary devices to laser illumination, in order to model and predict the behavior of more complex circuits. This paper presents measurements of the photoelectric currents induced by a pulsed laser on a triple-well Psubstrate/DeepNwell/Pwell structure dedicated to low power body biasing techniques. It reveals possible bipolar transistor activation at high laser power. This activation threshold revealed its dependence on laser power and wells biasing. Based on the measurements made during our experiments, an electrical model is proposed that makes it possible to simulate the effects induced by photoelectric laser stimulation.

Introduction

Photoelectric Laser Stimulation (PLS) is commonly used in failure analysis methodologies [1]. PLS generates electron-hole pairs in silicon, as the laser energy is greater than the silicon band gap. Our PLS experiments were carried out with a pulsed laser at 1064 nm wavelength. The active parts of the triple-well device (designed in STMicroelectronics 90-nm CMOS technology) were exposed through its backside (see figure 1).

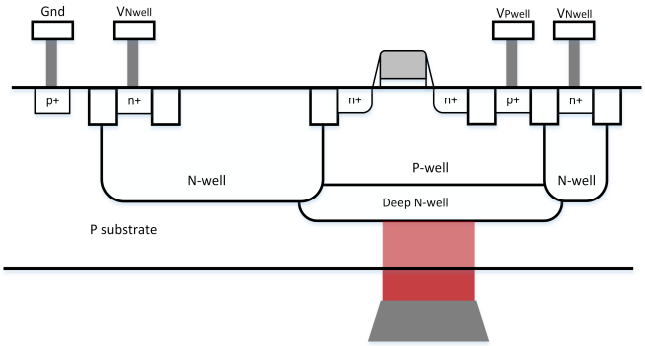


Figure 1: Triple-well structure under PLS representation.

The measurements were used to validate and calibrate the electrical model in order to create a fast and simulated SPICE solution under laser stimulation. This electrical model allows to simulate the response of an NMOS transistor in a triple-well structure to laser pulses in a very small amount of calculation time by comparison with physical experiments on laser equipment or TCAD simulation.
PLS generates electron-hole pairs in silicon, as the laser energy is greater than the silicon band gap. In silicon substrate or electric-field free areas these carries will diffuse and recombine rapidly. However, it has been shown [2], that inside a space charge region of a PN junction, electron-hole pairs will be separated by the internal electric field and then generate an optical beam induced current.
Furthermore, an electrical model of an NMOS under PLS has been studied in [3]. The novelty of this paper is that our model takes into account the parasitic bipolar transistor topologically added by the use of a triple-well for the body biasing techniques. With technology scaling down, performance and power consumption play an increasingly important role in logic circuit design. The body biasing technique presented in [4] and [5] is one well-known solution to adjust consumption and timing performance. This low power technique uses threshold voltage scaling by reverse or forward body bias. In 90nm CMOS technology, the body biasing range is +/- 400 mV applied on both NMOS and PMOS bulks (i.e. applied on the N and P wells).

The first electrical models of MOS transistors under pulsed laser stimulation reported in the literature were generally made of a current source which represents the photocurrent induced by the laser. In this paper we improved the electrical model already introduced in [3], [7] which takes into account the laser's spot size, laser power, pulse duration and the spatial parameters, location, geometry, wafer thickness and focus of the laser beam. Our major improvement is on the parasitic bipolar study and modeling.

This article begins by explaining the model of the PN junctions involved by a triple-well structure under PLS as well as parasitic bipolar effects. Second, the impact of body biasing techniques is studied. Finally, our model and electrical simulation method are proposed.

Triple well measurement and modeling

The study of each junction of our structure is a necessary step in the understanding of the phenomena involved by the laser beam illumination. The experiments were performed with a laser spot diameter of 1 µm, a laser shoot duration of 5 µs and a laser power between 0 and 250 mW. The Device Under Test (DUT) is a 10 x 1 µm NMOS in a 6 x 30 µm triple-well stand-alone structure (see figure 1 for a cross-sectional view of the triple-well structure). For our experiments, we search to understand the behavior of the triple-well structure. Thus in our DUT the NMOS transistor is ignored (not biased). In this condition, there are mainly two kinds of PN junctions which may give rise to a photoelectric effect (DeepNwell/Psubstrate junction and DeepNwell/Pwell junction). Therefore the first step is the study and the modeling of these PN junctions under PLS.

DeepNwell/Psubstrate junction

The laser spot was centered in the middle of the triple-well structure. The laser-induced photocurrent (see figure 8a) on the DeepNwell/ Psubstrate junction (Pwell not biased) varied linearly with the laser power as depicted in figure 2.

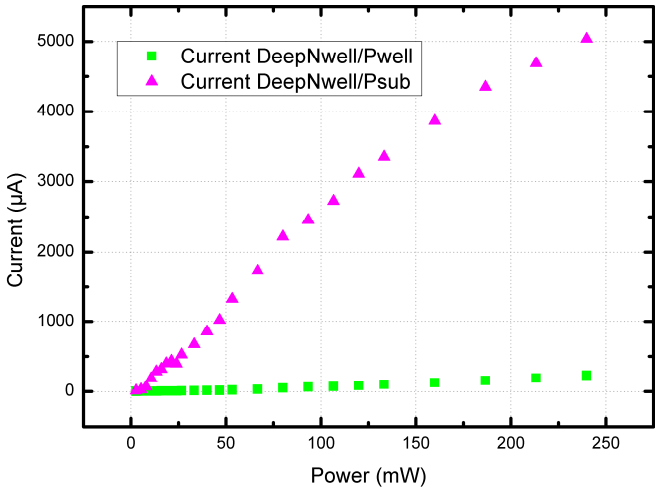


Figure 2: Current generated through the DeepNwell/Psub and DeepNwell/Pwell junctions.

Moreover, with the reuse of the model defined by [3], we know that the more the PN junction is reverse biased, the higher the induced current. For this junction, the maximum photocurrent amplitude used in our model induced by a laser pulse is:

$$I_{ph} = (a\,V + b)\;\alpha_{gauss}\;Pulse_{width}\;W_{coef}\;I_{ph\_z} \qquad (1)$$

where, V is the reverse biased voltage of the PN junction, a and b depend on the laser power, α_{gauss} is the sum of two Gaussian functions which take into account the spatial dependency, $Pulse_{width}$ considers the laser pulse duration dependency, W_{coef} is an exponential function allowing for the wafer thickness effect and I_{ph_z} is a curve function which considers the focus effect of the z axis of the laser lens:

$$\alpha_{gauss} = \beta\, e^{\left(\frac{-d^2}{c_1}\right)} + \rho\, e^{\left(\frac{-d^2}{c_2}\right)} \qquad (2)$$

$$Pulse_{width} = 1 - e^{\left(\frac{-t_{pulse}}{250\cdot10^{-9}}\right)} \qquad (3)$$

$$W_{coef} = e^{-0.001\,Wafer_{thickness}} \qquad (4)$$

$$I_{ph\_z} = (c_1 z^6 + c_2 z^5 + c_3 z^4 + c_4 z^3 + c_5 z^2 + c_6 z + c_7) c_8\, e^{\frac{-z^2}{20000}} \qquad (5)$$

where, d is the distance (in µm) between the laser spot and the center of the PN junction, t_{pulse} is the laser pulse duration (in second), $Wafer_{thickness}$ is the thickness of the wafer (in µm) and z is the laser lens distance (in µm) with $z = 0$ when focused on the active area. The other coefficients depend on the CMOS technology and laser lens.

In order to simulate this photocurrent effect, the sub circuit (see figure 3) which contains a voltage controlled current source was built. The current amplitude of the current source is described by (1) and the start and duration of the laser pulse is set by the laser_trigger signal.

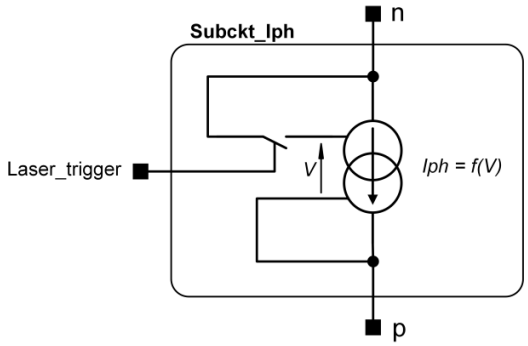


Figure 3: Electrical modeling of a PN junction under pulsed laser embedded in a sub circuit called Subck_Iph.

DeepNwell/Pwell junction

With identical laser settings, the photocurrent generated on the second DeepNwell/Pwell junction (Psub not biased) has a similar linear shape but attenuated by 25 to 100 on our measured power range (see figure 2). Thus, for equation (6) the model of this second interface, we add an attenuation coefficient γ = 50 on the model (1).

$$I_{phDeepNwellPwell} = \frac{1}{\gamma}(a\,V + b)\;\alpha_{gauss}\;Pulse_{width}\;W_{coef}\;I_{ph\_z} \qquad (6)$$

The sub circuit (called Subckt_Iph) is re-used on this second junction with the only difference being the current amplitude modeled by (6).

Pwell/DeepNwell/Psubstrate parasitic bipolar transistor

Once the behavior of the single PN junctions under PLS are understood and modeled, the phenomenon involved when the Pwell, DeepNwell and Psub are biased is studied. Both photocurrents described previously have for consequence to locally decrease the Pwell and Psub potential and increase the local Nwell potential due to the parasitic well and access resistors.

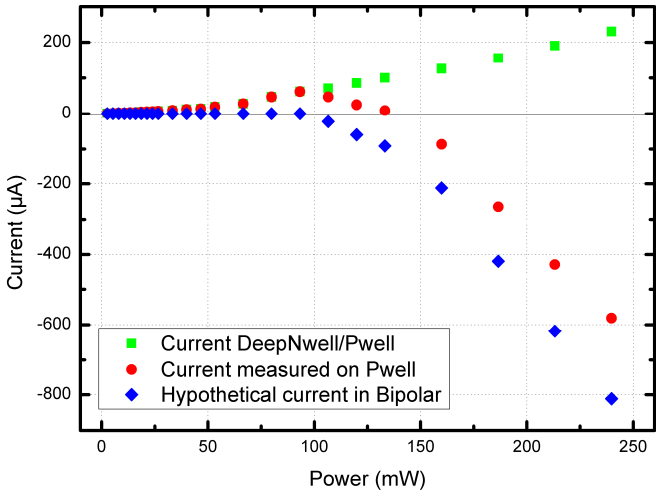


Figure 4: Current behavior on Pwell for parasitic bipolar transistor modeling.

Furthermore, figure 4 shows the current measured on the Pwell contact when Psub = 0 V, Nwell = 1.2 V and Pwell = 0 V. As the laser power is progressively increased, a linear photocurrent is generated at low laser power (0 to 90 mW) while we noticed a decrease of the current on Pwell for a laser power greater than 90 mW. When the photocurrent flowing into the Pwell and the DeepNwell induced a differential local voltage greater than 0.6 V due to the parasitic well and access resistors, then a current flows from Pwell to Psubstrate by the activation of the parasitic PNP bipolar transistor (Figure 5).

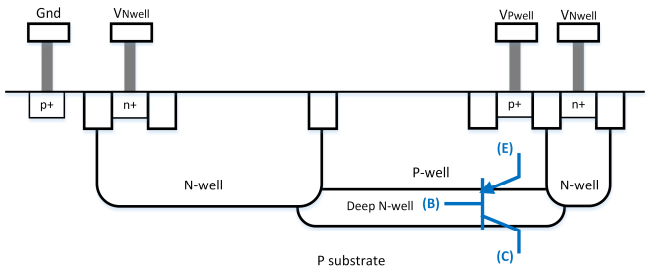


Figure 5: DUT structure with parasitic PNP bipolar representation.

For modeling this PNP activation effect, a preliminary study without PLS of the local potential was performed to characterize the current gain of this bipolar transistor. With our results and [6], we decided to define the model as a voltage-controlled current source, where the current amplitude is:

$$I_{bipPNP} = I_s \, exp^{\delta \frac{V_{EB}}{V_T}} \quad (7)$$

where, I_S is a constant used to describe the transfer characteristic of the transistor in the forward-active region (typically 10^{-14} to 10^{-16} A), δ is a modeling coefficient in order to fit the simulation and the measurements, V_T is the thermal voltage and V_{EB} is the voltage between Pwell and DeepNwell.
In order to simulate this bipolar effect, the sub circuit (see figure 6), which contains a voltage-controlled current source, was built. The current amplitude of the current source is described by (7).

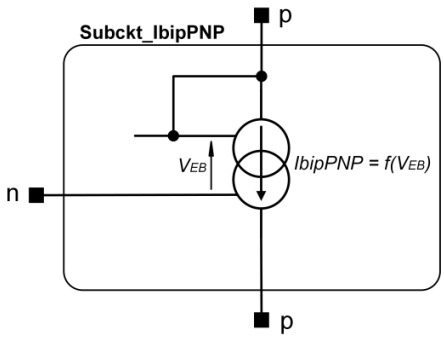
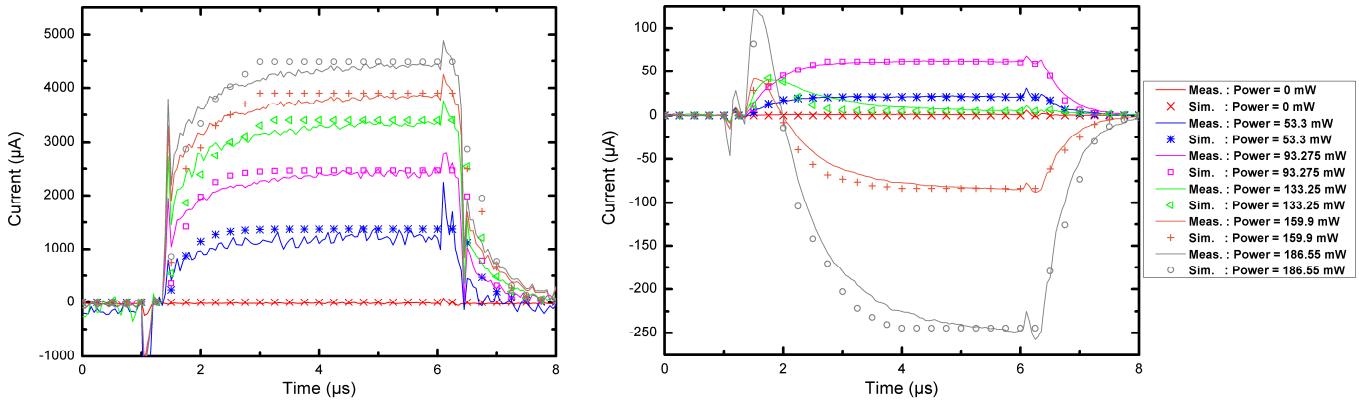


Figure 6: Electrical modeling of the Pwell/DeepNwell/Psubstrate parasitic PNP bipolar transistor in a sub circuit called Subck_Ibip.

Therefore our models of the PN junctions and parasitic bipolar transistors under PLS which take into account the position of the laser beam, the wafer thickness, the focus of the laser beam and the well biasing voltage will allow us to rapidly simulate the effects impacted by PLS on our DUT previously described.

Impact of body biasing techniques

The aim of the present work is to investigate the influence of Forward body biasing (FBB) and Reverse body biasing (RBB) conditions on the parasitic PNP bipolar transistor activation. For the DeepNwell/Psub junction, Psubstrate is always grounded, DeepNwell = 0.8 V in FBB and 1.6 V in RBB condition. Then, the photocurrent generated is more important in RBB than in FBB due to a higher junction reverse biasing. For a laser power = 93.275 mW, the photocurrent on DeepNwell/Psub = 2.5 mA in FBB condition and 2.9 mA in RBB condition. This trend is the same for the second DeepNwell/Pwell interface. In addition, for the maximum FBB condition Nwell = 0.8 V and Pwell = 0.4 V, the V_{EB} bipolar activation condition is closer. Figure 7 depicts the RBB and FBB impact on the Pwell current for different laser power values. As we expected, the FBB condition is a



(a) Psub current (b) Pwell current

Figure 8: Comparison of experimental and simulation results on Psub and Pwell current.

contribution of bipolar activation and the RBB condition limits this impact.

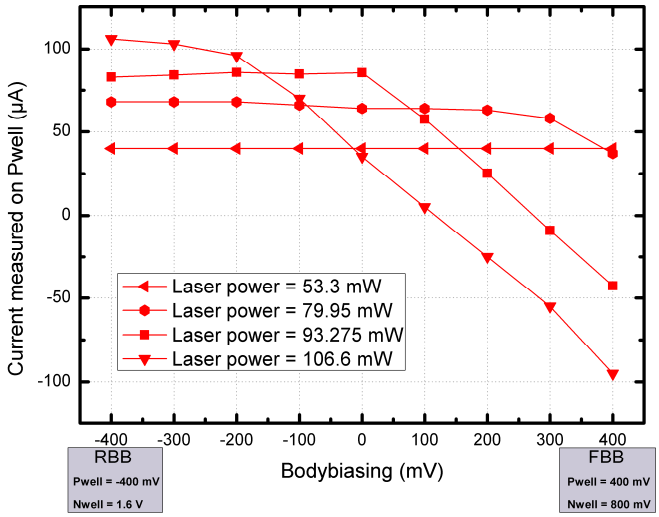


Figure 7: Body biasing impact on Pwell current.

Triple-well simulation

A proper post-layout SPICE simulation of a triple-well structure requires the addition of different parasitic diodes: Nwell/Psub diode, DeepNwell/Psub diode and DeepNwell/Pwell diode. Figure 9 shows the electrical simulation models of our DUT with the various photoelectric model effects we built. Photoelectrical current generated on PN junctions are modeled by *IphDeepNwellPsub* and *IphDeepNwellPwell* and the parasitic PNP bipolar transistor by *IbipPNP*. The various sub-circuits were tuned using electrical measurements in order to take into account laser power and body biasing variations. Measurement and simulation comparison results are displayed on figure 8 for Psub and Pwell currents. A good correlation is obtained by the model. The different modeling coefficients were tuned in order to fit perfectly with the measurements. A fast electrical simulation can provide a very accurate prediction of the DUT's behavior. Moreover, our model takes into account the spatial parameters, making it possible to draw 3D current cartographies based on the creation of a mesh on the structure's layout.

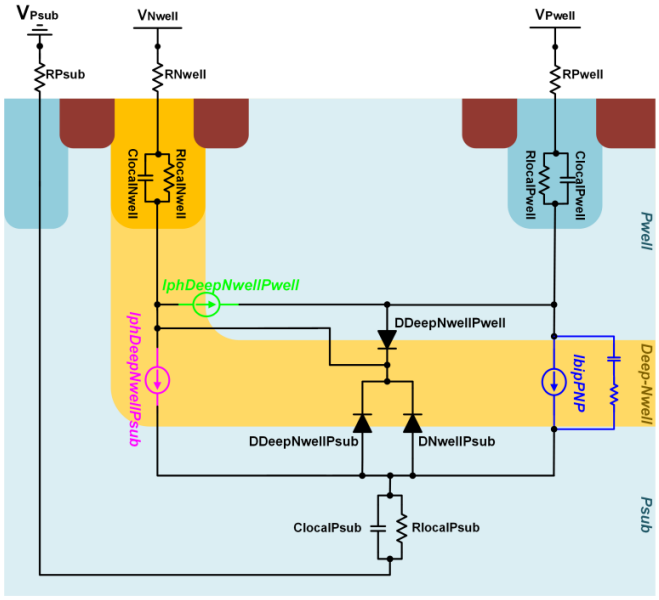


Figure 9: Triple-well test bench simulation with PLS models.

Conclusions

This paper describes an accurate triple-well electrical model that takes into account body biasing technique under pulsed laser in 90 nm CMOS technology. This model combines all various photoelectrical phenomena revealed by measurements during the PLS. The effectiveness of our approach has demonstrated a very good correlation between measurements and our model. In failure analysis, this proposed simulation technique may serve as a reference to detect defaults by comparison with a device under pulsed laser. It may also help localize specific defaults under FBB or RBB conditions.

Future work will consist in characterizing and modeling NMOS and PMOS transistors in triple-well technology. As a perspective, it will allow us to simulate the behavior of complex logic gates inside a triple-well process.

References

[1] A. Glowacki, S. K. Brahama, H. Suzuki, C. Boit. "Systematic characterization of integrated circuit standard components as stimulated by scanning laser beam", ISTFA 2010

[2] K. Haraguchi, "Microscopic optical beam induced current measurements and their applications", Proc. of 10th IEEE IMTC, vol. 2 issue pp.693-699, 1994

[3] A. Sarafianos, "Building the electrical model of the pulsed photoelectric laser stimulation of an NMOS transistor in 90nm technology", IRPS 2013

[4] D. Liu and Ch. Svensson. "Trading Speed for Low Power by Choice of Supply and Threshold Voltages", IEEE J.Solid-State Circuits, 28(1):lO-17, 1993

[5] A. Keshavarzi, S. Narendra, S. Borkar, C. Hawkins, K. Roy, and V. De, "Technology scaling behavior of optimum reverse body bias for standby leakage power reduction in CMOS IC's" in Proc. Int. Symp. On Low-Power Electronics and Design, Aug. 1999, p. 252.

[6] P. Gray, P. Hurst, S. Lewis, R. Meyer, "Analysis and Design of Analog Integrated Circuits"

[7] A. Sarafianos, "Building the electrical model of the pulsed photoelectric laser stimulation of an PMOS transistor in 90nm technology", IPFA 2013