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Jean-Max Dutertre, Rodrigo Possamai Bastos, Olivier Potin, Marie-Lise Flottes, Giorgio Di Natale, Bruno Rouzeyre

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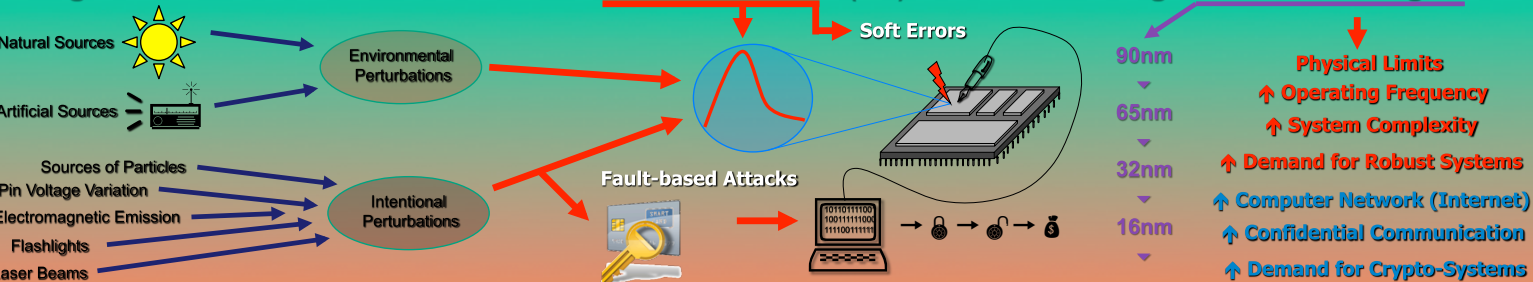
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# Design of Bulk Built-In Current Sensors to Detect Single Event Effects and Laser-Induced Fault Injection Attempts

J.-M. Dutertre<sup>1</sup>, R. Possamai Bastos<sup>2</sup>, O. Potin<sup>1</sup>, M.-L. Flottes<sup>3</sup>, G. Di Natale<sup>3</sup>, and B. Rouzeyre<sup>3</sup>

Bulk Built-In Current Sensors (BBICS) are fault detection mechanisms embedded in integrated systems. BBICS are able to monitor anomalous transient currents like the so-called single event effects induced by radiation or even malicious injection sources. This work reviews BBICS principles and introduces new sensor architectures that improve the transient-fault detection sensitivity. In addition, a test chip is presented for the validation of the sensor concept under the laser-induced effects.

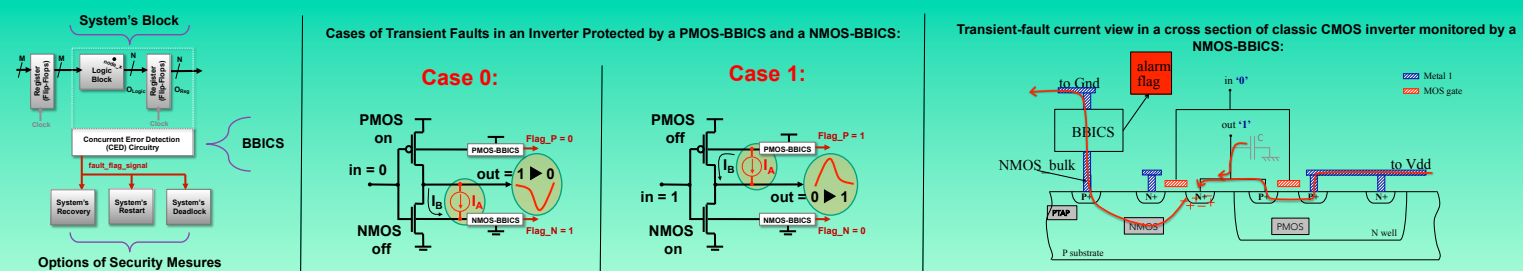
## Integrated circuits are more and more Transient-Fault (TF) sensitive through new technologies



## The today's trend in efficient protections against transient faults:



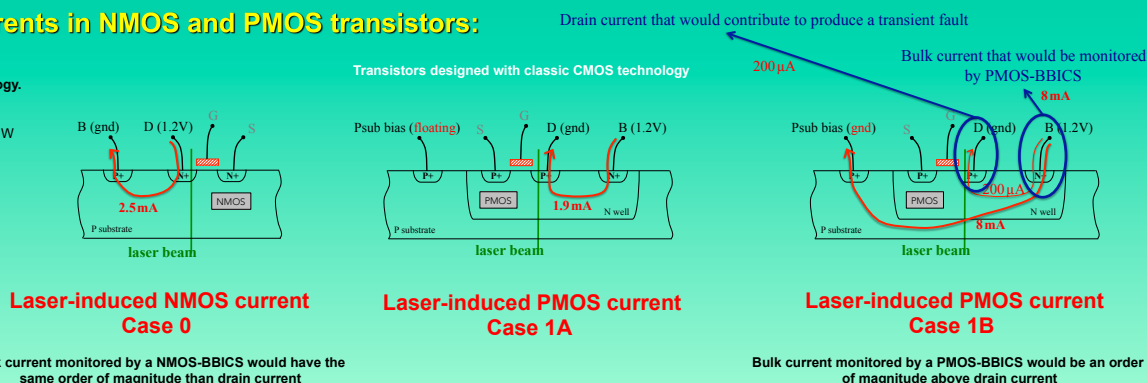
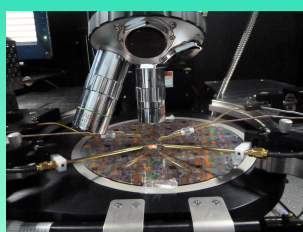
## Mitigation of Transient faults by using CED schemes based on Bulk Built-In Current Sensors (BBICS):



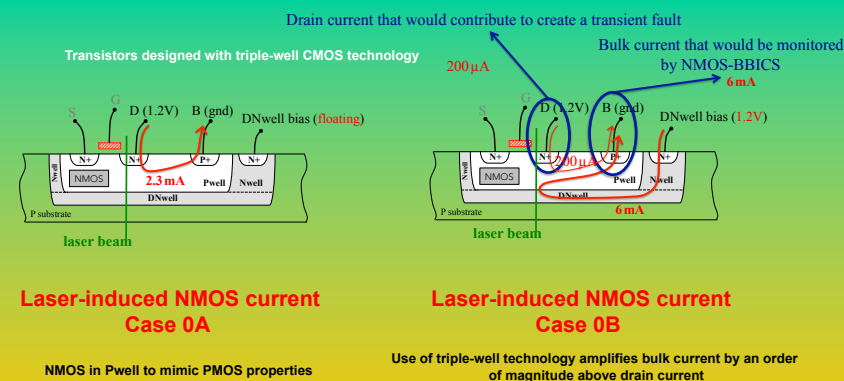
## Analysis of laser-induced currents in NMOS and PMOS transistors:

Test chip composed of single NMOS and PMOS transistors designed with classic and triple-well 90-nm CMOS technology.

Experiment settings: measure of laser-induced currents at  $\lambda = 1064 \text{ nm}$ , laser spot  $\varnothing = 5 \mu\text{m}$ , pulse duration =  $20 \mu\text{s}$ ,  $1.25 \text{ W}$



## Improving the transient-fault detection sensitivity of BBICS by using triple-well CMOS technology:



## Conclusions and Perspectives:

- + Laser-based experiments revealed:
  - 1) Classic PMOS transistors drive bulk currents much higher than drain currents, hinting efficient transient-fault detection sensitivity of PMOS-BBICS;
  - 2) Structural weakness in classic NMOS transistors that precludes NMOS-BBICS efficiently identifying anomalous bulk currents;
  - 3) Use of triple-well CMOS technology allows a distinction of the bulk current and improves the transient-fault detection sensitivity of NMOS-BBICS;
- + A 65-nm CMOS test chip is being tested to validate BBICS approach in such a technology.

Layout of 65-nm CMOS test chip with BBICS devices

