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Sensitivity Tuning of a Bulk Built-In Current Sensor for Optimal Transient-Fault Detection

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Abstract

Bulk Built-In Current Sensors (BBICSs) are able to detect anomalous transient currents induced in the bulk of integrated circuits when hit by ionizing particles. This paper presents a new strategy to design BBICSs with optimal transient-fault detection sensitivity while keeping low both area and power overheads. The approach allows increasing the detection sensitivity by setting an asymmetry in the flipping ability of the sensor's latch. In addition, we introduce a mechanism to tune the delay of the bulk access transistors that improves even more the BBICS detection sensitivity. The proposed design strategy offers a good compromise between fault detection sensitivity and power consumption; moreover it makes feasible the use of several CMOS processes.

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1. Introduction

Bulk Built-In Current Sensors (BBICS) were introduced to monitor the currents induced in the bulk of integrated circuits by ionizing particle hits. Such currents may create transient errors into the circuit's calculations. BBICSs are used to detect unusual bulk currents and to possibly trig recovery mechanisms to maintain the circuit's functionality.

This paper is organized as follows: Section 2 describes the principles underlying BBICSs. Moreover it reviews the architectures of the Tbulk BICS [1, 2] and also the one of a recently improved low power design [3]. The weaknesses of these designs are discussed to highlight the difficulties in adapting these designs to a CMOS 65-nm process. Section 3 describes the strategies proposed to obtain optimal fault detection sensitivity while keeping low both area and power consumption overheads. Section 4 draws a conclusion.

2. State-of-the-art

Integrated circuits (ICs) are known to suffer from Single Event Effects (SEEs) in harsh and radioactive environments. In this paper we consider two kinds of SEEs: Single Event Transient (SET) and Single Event Upset (SEU). In the following sub-sections we review the electrical phenomenon underlying SEEs, the BBICS principles, as well as the properties of two recent BBICS structures dedicated to the monitoring of the bulk currents induced by particle hits. Their main drawbacks are also reported.

2.1. Single Event Transients and related detection through bulk-current monitoring

When an ionic particle passes through silicon it generates electron-hole pairs along its path. These electrical charges generally recombine without any significant effect. However, the electron-hole pairs may be separated by the electric field found in a PN junction thus creating a transient current. Fig. 1 illustrates the inverter's case when its input is high (i.e. $in = 1$ and $out = 0$). In this configuration, the SEE sensitive part is the drain of the PMOS transistor,

which is in OFF state. Fig. 1 displays the cross section view of the inverter. The path taken by the generated transient current flows from the power supply (Vdd) through the biasing contact of the Nwell (the NTAP) and then through the PMOS drain. Next, it separates in two branches before reaching the ground. One part charges the inverter's output capacitance, while the other passes through the NMOS transistor, which is in ON state. When the whole electron-hole pairs have been drain away, the current ceases. The main effect is a transient alteration at the inverter's output from 0 to 1. This voltage transient, also known as SET, may thus propagate through the circuit logic creating soft errors in case of no logical, electrical or latching-window masking. Furthermore, whether a SET is induced directly in a memory element, the stored data may be flipped characterizing the so-called SEU (i.e. a soft error).

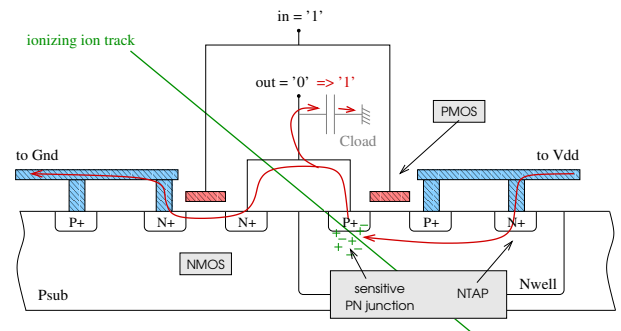


Figure 1: Single event transient mechanism: cross section view of an inverter.

Figure 2 gives a schematic view of the effect of a transient current induced by the ionic particle. A current source is used to represent the transient current generation. It illustrates a characteristic phenomenon of this transient current: it flows through the bulk of the struck sensitive transistor. BBICSs are designed to take advantage of this phenomenon. These sensors monitor the transistors' bulk currents, detect unusual currents and, consequently, the advent of SET or SEU. Note that NMOS transistors can be affected as well, however, for the sake of brevity we have only described the PMOS case and the BBICS' architecture dedicated to monitor these transistors.

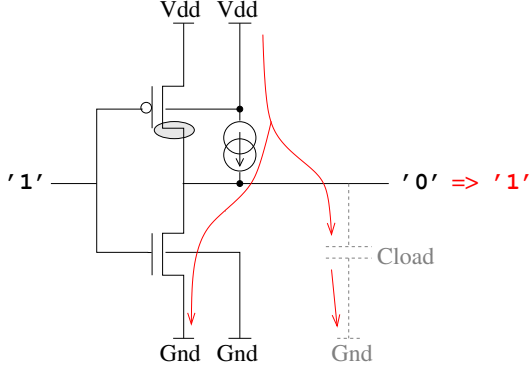


Figure 2: SET mechanism: inverter schematic outline.

2.2. BBICS principles

Bulk currents induced during normal operation of an IC are in the μA range; whereas particle-induced bulk currents have to be above some hundreds of μA to generate an SET on the related gate output.

Fig. 3 depicts the insertion of a BBICS between the bulk (the Nwell) of a PMOS transistor and the power supply. Note that the biasing at Vdd of the Nwell is provided by the BBICS. Hence, as illustrated, any transient current necessarily flows through the BBICS. The BBICS purpose is then to raise a warning flag indicating that the circuit's function may be affected.

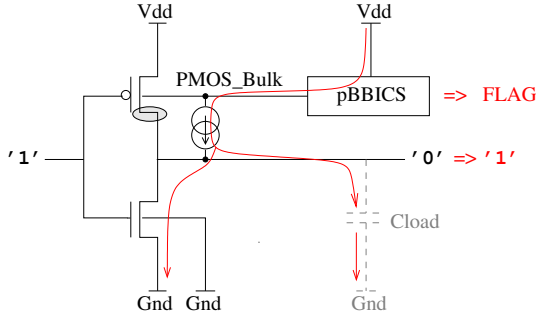


Figure 3: PMOS sensitivity monitoring with a pBBICS.

In Fig. 3, the BBICS used to monitor the Nwell of PMOS transistors is named a pBBICS. It also exists nBBICS dedicated to the monitoring of NMOS transistors. Even if pBBICS and nBBICS have different architectures they rely on the same principle, i.e. the monitoring of bulk currents.

2.3. The Tbulk BICS and its most recent improvement

E.H. Neto et al. have introduced the first BBICS [1]. We review in the next subsection the main char-

acteristics of their most recent design, the Tbulk BICS [2]. We also review a recent low-power improved BBICS proposed in 2012 [3].

2.3.1. The Tbulk BICS

Fig. 4 depicts the architecture of a Tbulk BICS used to monitor PMOS transistors. The Tbulk BICS makes use of trimming transistors in order to cope with ICs' variability. Nevertheless, we do not analyse their effect in details for the sake of simplicity.

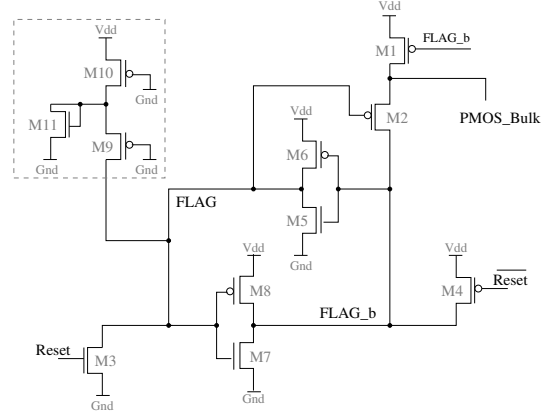


Figure 4: Tbulk BICS architecture for PMOS monitoring [2].

The core part of this Tbulk BICS is a memory latch made of two cross-coupled inverters (transistors M5-M6 and M7-M8). In normal operating conditions, node *FLAG* is at low level while node *FLAG_b* is high. *FLAG_b* goes low to indicate the detection of an unusual bulk current. The BBICS connection to the Nwell of the monitored transistors (node *PMOS_bulk* in Fig. 4) is used as a bias contact to Vdd through the ON transistors M2 and M8.

When a particle hits the device, the induced current flows to the Nwell (i.e. the bulk) from the Tbulk BICS through *PMOS_bulk* and M2. It discharges the capacitance of node *FLAG_b* (a counterbalancing charging current also flows from Vdd through M8 to *FLAG_b*). As a result, the voltage of node *FLAG_b* decreases to the point where the BBICS' core latch flips. *FLAG_b* going low indicates an SEE detection. In the meantime, M2 switches to OFF state and M1 to ON state respectively. The latter ensures a proper biasing of the Nwell to Vdd.

A key point in designing a BBICS is to obtain a sensitivity level lower than the level of appearance of SEEs. The purpose of transistors M9, M10 and M11 is to weaken the core latch stability to that end.

2.3.2. BBICS with low-power sleep-mode

The work in [3] proposes a BBICS architecture (depicted in Fig. 5) that overcomes with the main drawback of the Tbulk BICS architecture: the huge static power consumption due to transistors M9, M10, and M11 illustrated in Fig. 4. In fact, these three transistors act to improve the detection sensitivity of the sensor by setting a small permanent voltage offset at *FLAG* node. It makes easier the flipping ability of the Tbulk BICS latch; however it also considerably increases the sub-threshold leakage current of transistors M7 and M10. Moreover, simulation results presented in [3] show that the Tbulk BICS without trimming transistors suffers from overheads in area (above 55%) and in power consumption (higher than 100%) when compared to an unprotected reference circuit. Furthermore, the BBICS version in [3] introduces transistor M9 (detailed in Fig. 5) as a low-power sleep-mode feature that can be enable in case of the system is left on standby. Results from [3] highlights overheads of 25% and 40% respectively in area and power consumption. If the sleep-mode is active, the power overhead is reduced to 25%.

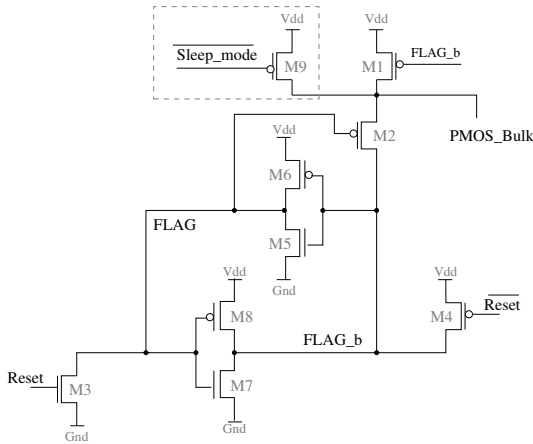


Figure 5: PMOS BBICS with low-power sleep-mode [3].

2.4. Adequacy with different CMOS technology nodes

The structures of the Tbulk BICS (Fig. 4) and its relative low-power version (Fig. 5) were designed by using 32-nm CMOS predictive technology models [4]. In order to produce a test chip, we have analysed the adequacy of the architecture in Fig. 5 for use with a commercial 65-nm CMOS technology. The monitoring capability of this pBBICS was found below the minimum SEE detection sensitivity of the process. An analysis of the design simulation results showed

that any decrease in the voltage of node *FLAG_b*, which is mandatory to flip the BBICS' core latch, also made transistor M1 switching progressively to ON state. Hence, it gives rise to a competition effect between two component of the bulk current, which will pass through transistors M1 and M2. Consequently, the voltage of node *FLAG_b* is not able to go down the threshold voltage of transistor M6. Fig. 6 illustrates such a scenario in which the bulk current (i.e. $I_{\text{pos_bulk}}$), the currents passing through M1 and M2 (i.e. $I_{\text{ds_M1}}$ and $I_{\text{ds_M2}}$), and the voltages of *FLAG_b* and *FLAG* are drawn.

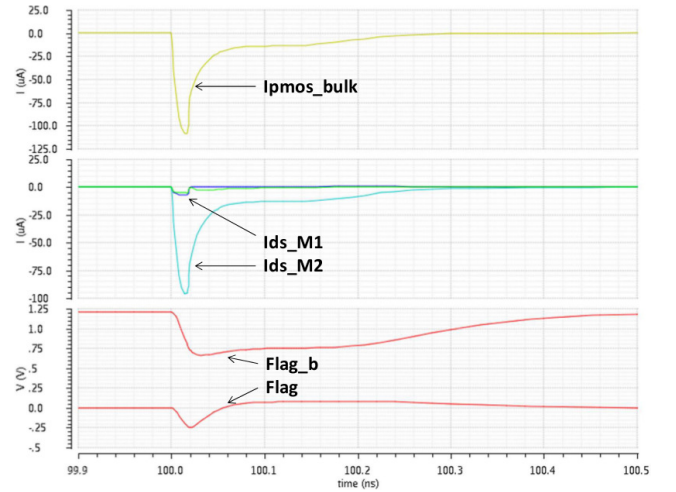


Figure 6: A 65-nm CMOS technology-based case study of Fig. 5 scheme showing the insufficient discharge of *FLAG* node to register the occurrence of a SET.

This study shows that an additional modification of the low-power BBICS is mandatory for achieving proper SEE detection in the CMOS 65-nm technology.

3. Improved BBICS design for optimal transient-fault detection in 65-nm technology

3.1. Proposed architecture

The original Tbulk BICS' sensitivity was enhanced by introducing an asymmetry in its core latch (transistors M9 to M11 in Fig. 4). The downside was an increase of its static power consumption.

We used an alternative unconventional approach that has a significant smaller effect on the power consumption (similar to that of the BBICS of [3]): the use of transistors with low and high thresholds voltage (hereafter denoted LVT and HVT respectively)

in place of standard ones. These three types of transistors are normally provided by most of commercial technologies. An LVT (HVT resp.) transistor has a highest (lowest resp.) current driving capability in ON state and passes from OFF to ON state more (less resp.) rapidly. Consequently, an inverter made of one LVT NMOS and one HVT PMOS has an asymmetrical behaviour: its output changes more easily from 1 to 0, than from 0 to 1. Respectively, the output of an inverter made of one HVT NMOS and one LVT PMOS change more easily from 0 to 1, than from 1 to 0. We used these two inverters features to increase the ability of the core latch to flip when a bulk current appears. We also used an LVT transistor for M2 and an HVT transistor for M1. Hence, the competition effect between the currents of M2 and M1 is modified in favour of M2's current, which increases the detection sensitivity by helping $FLAG_b$ voltage to diminish. A reinforcing effect due to the timing of the commutations of M1 and M2 was also obtained thanks to an adequate control of the switching time from ON to OFF and OFF to ON states of these access transistors. In fact, the M2 switch is tuned to open (from ON to OFF) only after $FLAG_b$ voltage has decreased enough to flip the BBICS latch. Further, the transition of M1 from OFF to ON in order to replace the PMOS bulk to Vdd is done just after the switching of M2.

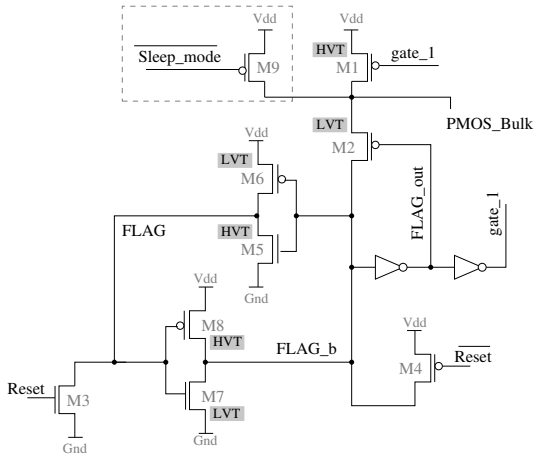


Figure 7: CMOS 65-nm improved pBBICS.

Our architectural solution uses a two inverters chain as depicted in Fig. 7. The chain input is connected to $FLAG_b$, its intermediate node ($FLAG_out$) is connected to M2's gate, and its output to M1's gate. This new architecture ensures that the command of M1 and M2 is postponed after the detection

of any bulk current.

3.2. Simulation results

For the purpose of both setting a sensitivity target and tuning the sizes of the BBICS' transistors, a first set of simulations was run on a chain of ten inverters. We used the smallest sizing for the NMOS and PMOS of the inverters: $L_{NMOS} = L_{PMOS} = 60nm$, $W_{NMOS} = 200nm$, $W_{PMOS} = 280nm$. The PMOS' bulk was connected to a pBBICS and the NMOS' bulk to an nBBICS. At this stage, the circuit's parasitic resistances and capacitances were not considered. On simulation basis, the minimal bulk current pulse on PMOS that gives rise to an SET or an SEU was determined to $130\mu A$ amplitude at 50ps duration (respectively $99\mu A$ amplitude at 50ps duration on NMOS bulk). Fig. 8 displays the successful detection of an SEE transient current ($147\mu A@50ps$) on a PMOS of the inverters chain (identical to the pulse used for the simulation results reported in Fig. 6). $FLAG_b$'s voltage is drawn below the switching threshold of the pBBICS by the SEE transient current. Consequently, the pBBICS flips and the alert signal $FLAG_out$ goes high.

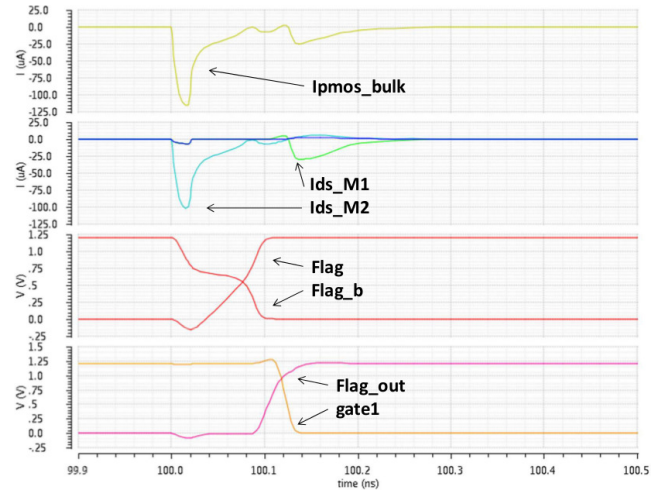


Figure 8: Improved pBBICS waveforms during SEE detection.

Similar simulations were also run to ascertain that the sensitivity target was reached in case of SEE transient current on an NMOS: the monitoring nBBICS raised successfully its alarm flag. As we highlighted in section 2.4, the architecture of the low-power BBICS was not able to reproduce the minimum SEE detection sensitivity of the CMOS 65-nm process by using its SVT transistors. Table 1 draws a comparison be-

tween these two BBICS architectures in terms of SEE detection capability and area.

These simulations were run for three corners of the technology: Typical-Typical, Fast-Fast, and Slow-Slow (TT, FF, and SS hereafter). The improved BBICSs passed successfully these tests contrary to the low-power sleep-mode BBICSs.

Table 1: Area and detection capability of BBICS cells: comparison between low-power sleep-mode [3] and improved BBICS

improved BBICS		
Type	Area	SEE detection (65-nm process)
pBBICS	$12.1\mu m^2$	yes
nBBICS	$11.3\mu m^2$	yes
low-power sleep-mode BBICS [3]		
Type	Area	SEE detection (65-nm process)
pBBICS	$10.5\mu m^2$	no
nBBICS	$10.5\mu m^2$	no

We have also assessed the efficiency of the improved pBBICS and nBBICS for different lengths of the monitored inverters chains. The corresponding simulations were run at typical conditions (TT corner) for a pulse duration of 50ps. Simulation results in terms of sensitivity threshold (the minimal transient current pulse sufficient for raising the BBICS' flag) and SET threshold (the minimal transient current pulse that results in an SET propagation from the input of the inverters chain to its output) are reported in table 2 for chains of 10, 30 and 50 inverters.

Table 2: Sensitivity and SET occurrence thresholds of the improved pBBICS and nBBICS versus the length of the monitored inverters chains - Simulation results for the TT corner and a pulse duration of 50ps

pBBICS			
# of inverters	10	30	50
Sensitivity threshold	$76\mu A$	$113\mu A$	$148\mu A$
SET threshold	$130\mu A$	$133\mu A$	$135\mu A$
nBBICS			
# of inverters	10	30	50
Sensitivity threshold	$87\mu A$	$93\mu A$	$118\mu A$
SET threshold	$99\mu A$	$101\mu A$	$102\mu A$

The sensitivity threshold increases with the number of monitored inverters. However, it remains below or close to the SET threshold until 50 inverters. Given the size of an inverter cell, $1.56\mu m^2$, the area

of the 50 inverters chain is $78\mu m^2$. Thus the area overhead due to both pBBICS and nBBICS is 30% which is similar to the overhead reported in [3].

3.3. Implementation

3.3.1. Design of a test vehicle

A test vehicle was designed in 65-nm CMOS technology to ascertain on experimental grounds the validity of the improved BBICS architecture. The test chip embeds various patterns of inverters chains monitored by pBBICS and nBBICS. This subsection reports electrical simulations that takes into account the parasitics elements of the standard cells in the target 65-nm CMOS technology. Fault-injection simulations were performed by using the technology's smallest inverter in order to analyse the minimum transient-fault profiles. Thereby, we inject a double exponential current source on the technology's lowest capacitance (i.e. on the node between two inverters with minor dimensions). The injected current must create a minimal voltage shape able to propagate through the technology's smallest inverter and to switch the output level of the smallest flip-flop. In accord with the description of the injection current source presented in [5], process and temperature corners were verified. Results for a target circuit compounded of 2 chains of 10 inverters protected by the proposed BBICS are summarized in table 3. For an injected current profile with a time rise $T_r = 8.2ps$, a time width $T_w = 124ps$ (measured at the half amplitude of the current), and a time fall $T_f = 330ps$, the minimum transient-fault profiles that are detectable by the BBICS are presented in terms of the minimum charges Q_{min} and the minimum current peaks I_{peak} that provoke a successful indication of fault.

3.3.2. Impact on standard cell design

The use of BBICS usually goes along with a huge re-design work: the adjustment of the standard cells in order to disconnect their bulk biasing contacts from the power supply and ground and to connect them to the BBICS's inputs. However, the CMOS 65-nm technology we used to design our test vehicle has an interesting feature: its standard cells do not embed any biasing contact. The biasing of the circuit's bulks is provided by dedicated fillers which are interspersed among the standard cells. Figure 9 - (a) depicts the layout of those biasing fillers: the Nwell (respectively the P substrate) is biased to Vdd (resp. to the ground) through the NTAP (resp. the PTAP)

Table 3: Minimum Detectable Transient-Fault Profile

	Corner	$I_{peak}(\mu A)$	$Q_{min}(fC)$
nBBICS	FS 80°C	84.5	14.3
	FS 0°C	109.4	18.5
	TT 27°C	112.1	18.9
	SF 0°C	131.7	22.2
	FF 80°C	53.7	9.2
	Corner	$I_{peak}(\mu A)$	$Q_{min}(fC)$
pBBICS	FS 80°C	121.3	20.9
	FS 0°C	148.7	25.3
	TT 27°C	126.6	21.5
	SF 0°C	119.5	20.3
	FF 80°C	67.3	11.6

and a contact (CON) to the metal 1 (MET1) supply rail. Thus, the only cell to be re-designed is the biasing filler. Figure 9 - (b) shows the layout of the new biasing filler used to connect the bulks of the monitored cells to the BICCSs. The contacts (CON) between the power rails and the NTAP and PTAP have been removed (their shapes were also slightly modified). New contacts have been added with corresponding metal 1 accesses to pBBICS's *PMOS_bulk* and nBBICS's *NMOS_bulk* nodes (see fig. 3 as an illustration).

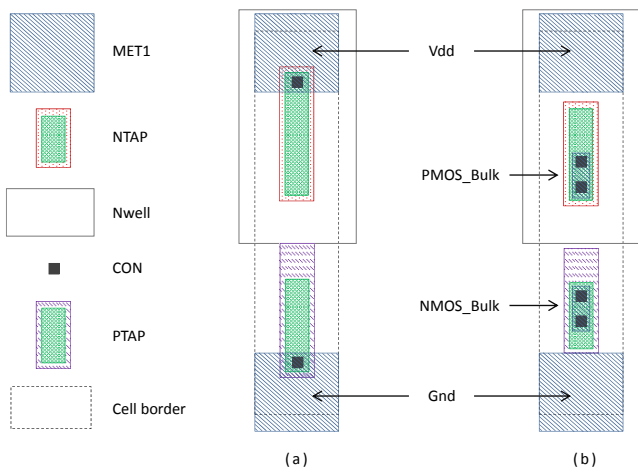


Figure 9: Standard cell biasing filler (a) and BBICS biasing filler (b)

4. Conclusion

We propose an improved BBICS dedicated to optimal fault detection. We use an unconventional approach to increase the detection sensitivity by in-

roducing an asymmetry in the flipping abilities of the BBICS' core latch. This behaviour was obtained thanks to the use of low and high threshold voltage transistors. The corresponding area overhead was estimated to 30%, a figure similar to a previous architecture [3]. The proposed principles are general enough to be easily adapted to any design implemented with recent CMOS submicron processes while guaranteeing low area and power overheads. Furthermore, the chosen technology allows to keep unmodified the standard cells, which simplified the design work necessary to use BBICS.

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