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Abstract— **This paper presents measurements of pulsed photoelectrical laser stimulation of an NMOS transistor in 90nm technology. The laser power was able to trig the NPN parasitic bipolar Drain/Psubstrate/Source. An electrical model is proposed in order to simulate effects induced by the laser. Results extracted from the electrical simulator are compared to measurements.**

Keywords-component; NMOS transistor; pulsed PLS; 1064nm wavelength; parasitic bipolar transistor.

I. INTRODUCTION

A laser beam passing through silicon creates electron-hole pairs along its path as a result of energy absorption: the so-called photoelectric effect. Failure analysis (FA) methodologies make an extensive use of laser stimulation techniques. In this paper, we present an electrical model of the backside Photoelectric Laser Stimulation (PLS) of an NMOS transistor in 90nm technology. We used a pulsed laser at 1064nm wavelength to conduct the PLS experiments. The obtained measurements were used to validate and tune the model. This electrical model makes it possible to simulate the response of an NMOS transistor to laser pulses in a very small amount of calculation time by comparison with real experiments on laser equipment, or TCAD simulations. Thus, a new model has to be built for any technology improvement. Such models are intended to reduce the time passed on laser equipments. This work presents the electrical model (thanks to ELDO, the SPICE simulator from Mentor Graphics [1]), of the effect of a laser pulse applied to the backside of an NMOS transistor in 90nm CMOS technology. This model is valid for laser power ranging from 0 to ~2W. In order to validate and correlate the model, measurements on NMOS transistors under laser illumination at a wavelength of 1064nm were performed with a laser equipment.

Moreover TCAD analyses are needed, in order to well understand the phenomenon involved when an NMOS transistor is under PLS. TCAD takes into account the complex flow of semiconductor fabrication steps leading to detailed information on geometric shape and doping profile distribution of a semiconductor device in scope (like a MOS transistor) [2] to model its behavior. Three-dimensional simulation is computationally intensive and requires very long simulation times. Thus, only two dimensional (2D) TCAD simulations have been considered in this paper. We assume that the third space dimension does not significantly affect the behavior of the fundamental mechanisms involved in the following results, as the third dimension of the device (width of the transistor) is taken as long enough to neglect edge effects (W=10µm). The laser waves used in all TCAD simulations were in every case, a plane wave which illuminates the whole backside of the studied devices.

Moreover, comparisons between measures and simulations will rather be qualitative than quantitative because TCAD simulations are first used as an analysis tool of physical laws effects inside a structure, and should be accurately calibrated before any quantitative analysis. Electrical measurements associated with Finite Element Modeling software are the tools necessary to understand and model PLS impact on NMOS transistors.

Former electrical models of NMOS transistors under pulsed-laser stimulation were generally made of a simple current source which represents the photocurrent induce by the laser [3]. We have already introduced electrical models for continuous illumination at small laser power (below ~100mW), which only consider photoelectrical effects [4], [5], [6], [7]. The novelty of the model presented in this paper is that it takes into accounts the laser's parameters (i.e. spot size, power, pulse duration, etc.), spatial parameters (i.e. the spot location, NMOS' geometry, wafer thickness, focus of the laser beam, etc.), the NMOS' bias, in addition to the possible activation of the NMOS' bipolar parasitic transistor at higher laser power. Besides, the model was calibrated for each laser settings (power, spot size, location, etc.).

This article is organized as follows. Section 2 reports both measurements made on silicon and TCAD simulations. It permits to draw the electrical model of a PN junction under PLS. This model is used in turn to build a complete electrical model of an NMOS transistor under PLS, thanks to measurements made for different laser and NMOS parameters. This model offers the ability to draw 3D cartographies of an NMOS under pulsed laser for FA purposes as reported in section 3. These electrical cartographies are compared to measurement. Finally, our findings are summarized in the concluding section 4 with some perspectives.

II. SILICON MEASUREMENT UNDER PLS AND ASSOCIATED ELECTRICAL MODEL

In an NMOS transistor there are mainly two PN junctions which may give rise to a photoelectric effect if exposed to a laser beam: the Drain/Psubstrate and Source/Psubstrate junctions. Therefore a first step toward building the electrical model of NMOS transistors under pulsed PLS is the study and the modeling of the PN junctions under pulsed laser. In order to reach this goal, the Device Under Test (DUT) used is the N+ diffusion on Psubstrate of an NMOS transistor (W=L=10µm) embedded in a test structure designed in STMicroelectronics 90nm technology.

A. N+/Psubstrat junction

The study of the N+/Psubstrate PN junction under PLS is a necessary step in the comprehension of the phenomena involved when a pulsed laser stimulates the backside of an NMOS transistor.

1) Beam centered on the component

In order to well model the effect of PLS on a PN junction the laser spot must firstly be centred in the middle of the junction.

a) Measurements and TCAD simulation

The test experiments were performed with a 20X lens (which delivers a spot size of diameter equal to 3.25µm). The laser spot was located in the middle of the Drain/Psubstrate junction (See Figure 1). The focus was made on the active zone. The laser power at the output of the chosen 20X lens was adjustable between 0 and 1.25W. Moreover, the pulse width used for the measurements was equal to 20µs. This value was used in order to analyze the PLS effect during a stationary regime. The main characteristics of the experiment are presented on figure 1. The red spot represents the location of the laser beam on the Drain/Bulk PN junction. The bias applied to the structure was the following: the drain potential was adjustable between 0V and 1.2V, and the Psubstrate was grounded. Gate and source are left floating, in order to focus the study only on the n+/Psubstrate junction (Drain/Bulk junction) of the NMOS transistor.

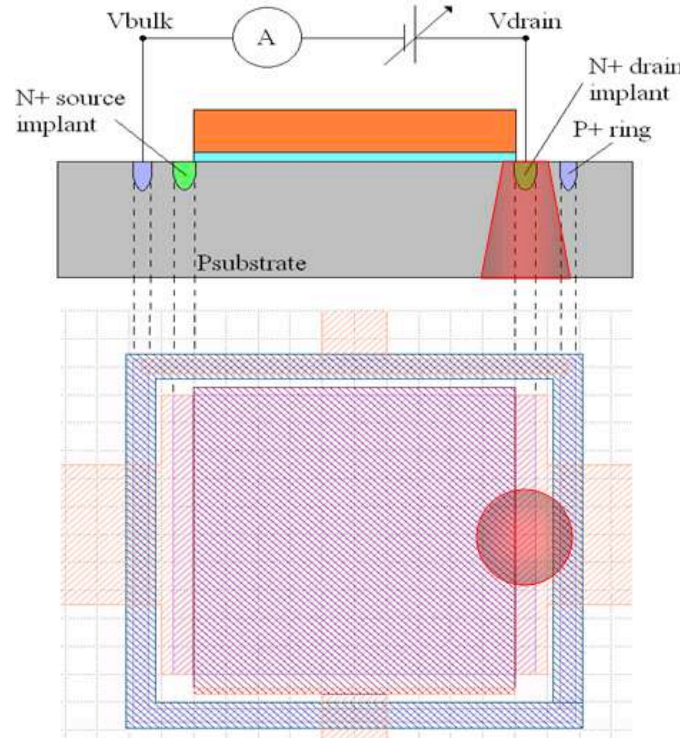


Figure 1. Study of the N+/Psubstrate diode of an NMOS transistor.

The I(V) characteristics depicted on figure 2 were obtained for various laser power according to the aforementioned settings. For each point the photocurrent was measured during the laser pulse. For a given laser power, more the PN junction is reverse biased and more the electrical field between the two electrodes increases, which induces a higher photoelectric current. This effect is amplified when the laser power is increased.

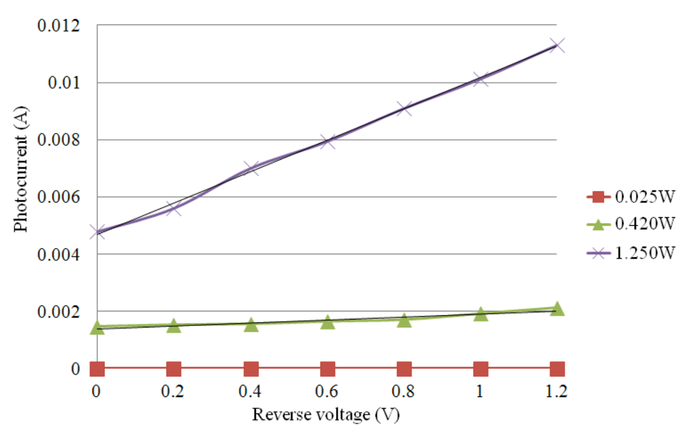


Figure 2. I(V) characteristics of the PN junction under pulsed laser for different laser powers.

Moreover, for validation purposes, TCAD simulations were ran on a N+/Psubstrate junction. The aim of this simulation was to reproduce the photocurrent induced in the Space Charge Region (SCR) of the device. In this work, Synopsys simulation tools are used and especially Sentaurus Device Editor (SDE) for grid generation and SDevice for device simulation. The simulated device is a Drain/Psubstrate (or Source/Psubstrate) junction of an NMOS transistor from a STMicroelectronics 90nm CMOS technology (See fig. 3). Advantages to proceed this way are that a single structure is generated and information about phenomena taking place in the PN junctions present in an NMOS transistor is obtained.

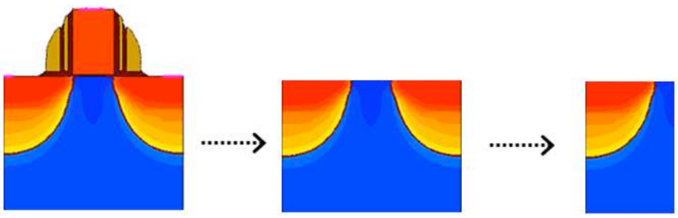


Figure 3. Structure used for TCAD simulation of the PN junction.

Current versus voltage characteristics of the junction were simulated as a function of the laser power. Due to calculus convergence problem, the level of the laser power simulated in TCAD is very low in comparison with measurement. At these laser power, the increase of the photocurrent versus the reverse bias is negligeable. However, it is possible to notice the increase of the photocurrent with the laser power.

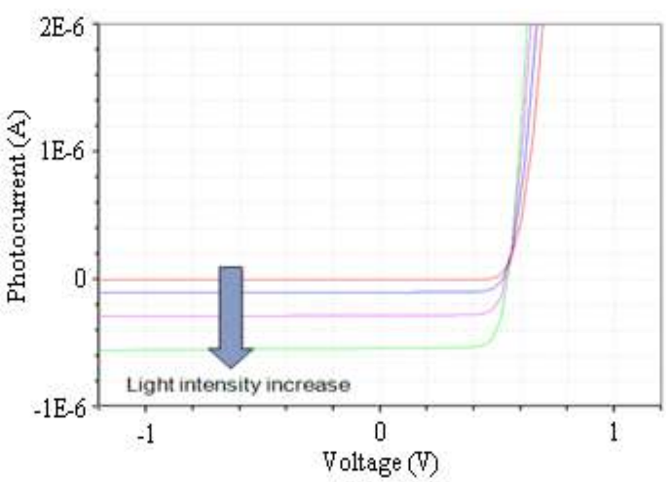


Figure 4. I(V) characteristics of the PN junction under pulsed laser for different laser power extracted from TCAD simulations.

b) Electrical model

In first approximation, it is possible to highlight the fact that the photocurrent induced in a reverse biased PN junction by a laser pulse could be approximated by a first order polynomial function (1):

$$I_{ph} = a \times V + b \tag{1}$$

Figure 5 displays the graph presenting the evolution of coefficients *a* and *b* from equation (1) versus the laser power.

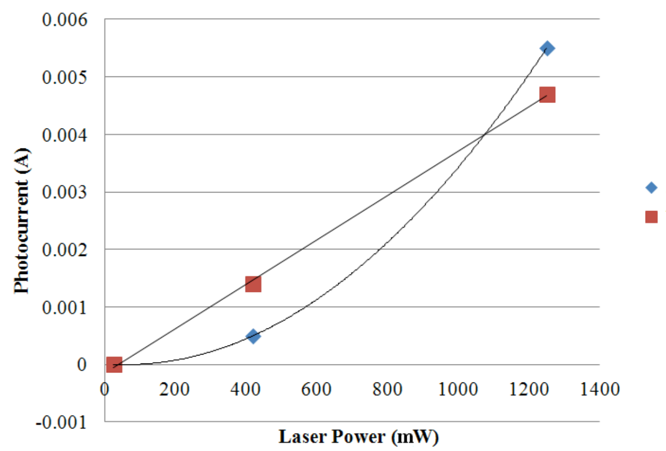


Figure 5. Coefficients a and b from equation (1) versus the laser power.

Therefore it is possible to approximate coefficients *a* and *b* by two functions which depend of the laser power P_{laser} expressed in W:

$$a = p \times P_{laser}^{\ 2} + q \times P_{laser} + r \tag{2}$$

$$b = s \times P_{laser} \tag{3}$$

Coefficients *p*, *q*, *r* and *s* are expressed in Table I.

TABLE I. VALUES OF COEFFICIENTS P, Q, R AND S.

Coefficient	Value
p	$4E^{-9}$
q	$-5E^{-7}$
r	$9E^{-6}$
s	$4E^{-6}$

The first step in order to simulate an NMOS transistor under pulsed laser stimulation is to well model its effects on the N+/Psubstrate junction.

According to the previous paragraph, it is possible to approximate the photocurrent generated in a PN junction during a laser pulse versus the bias applied to its two electrodes with equation (1), (2) and (3).

In order to simulate this effect, a sub circuit (called *Subckt Iph_nplus_psub*) which contains a voltage controlled current source was created. (See figure 6). The laser_trig signal is used to set the start and duration of the laser pulse.

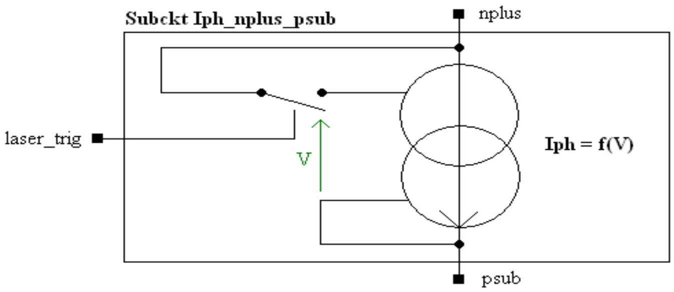


Figure 6. Electrical modeling of a PN junction under pulsed laser embedded in a sub circuit called Subckt_Iph_nplus_psub.

The value of the current source *Iph* is set by the same equation than expressed in (1) with equations (2) and (3) which coefficients are expressed in table I.

Figure 7 reports both simulation and experimental results. It highlights the very good correlation obtained.

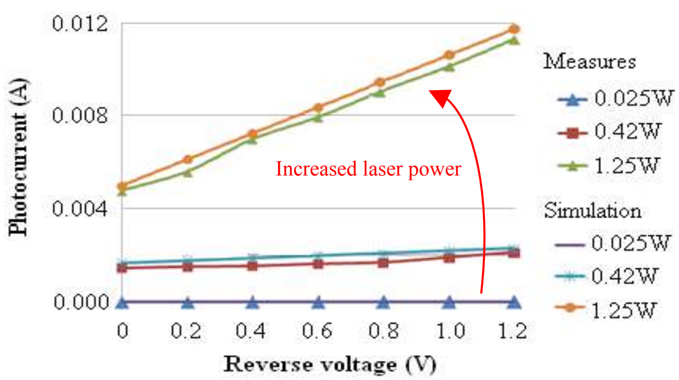


Figure 7. Comparison between measurement and electrical model of a PN junction under PLS for different laser power – I(V) characteristics.

2) *Study of the spatial dependence*

a) *Measurement*

The distance between the laser spot and the PN junction has a strong impact on the value of the generated photocurrent. In the following, this effect is studied for a N+/Psubstrate junction.

When the laser beam is centered on the PN junction (Drain/Psubstrate junction of an NMOS transistor), the induced photocurrent is maximum; as the laser beam is moved outside the junction the value of the photocurrent decreases.

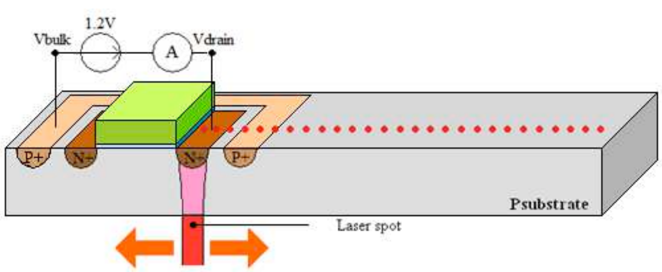


Figure 8. Schematic presentation of the experiment in order to know the spatial effect of the laser on a PN junction.

In order to model the spatial dependence effect on a Drain/Psubstrate junction (N+/Psubstrate junction), an NMOS transistor with long channel (W=L=10µm) was used. The measurements were made with the drain at 1.2V, the Psubstrate bias grounded, and the two other electrodes left floating. The laser spot was moved on a line from the center of the junction to a distance of 300µm. (See Fig. 8). For each step, the photocurrent was measured. This experiment was conducted for the three lenses of our laser equipment (5X, 20X, and 100X). The obtained photocurrent versus distance curves are depicted on figure 9 after normalization according the maximum photocurrent. Their shapes exhibit a Gaussian-like behavior.

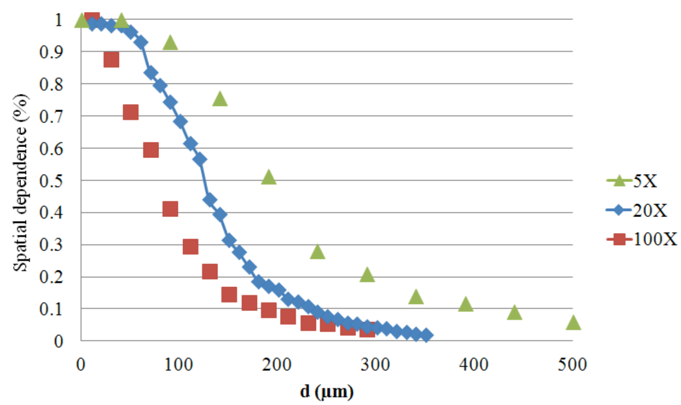


Figure 9. Spatial dependance of the induced photocurrent for the three different lenses of our laser equipement.

It makes it possible to extract a mathematical model based on the sum of two Gaussian functions (4), where *d* is the distance between the spot and the closest edge of the junction expressed in micrometer:

$$\alpha_{gauss}(d) = \beta \times \exp\left(-\frac{d^2}{c_1}\right) + \gamma \times \exp\left(-\frac{d^2}{c_2}\right) \qquad (4)$$

For each lens, the coefficients β, γ, c_1 and c_2 were found different (see Table II).

TABLE II. COEFFICIENTS OF THE GAUSSIAN FUNCTION (4) FOR THE DIFFERENT LENSES OF OUR LASER EQUIPEMENT FOR THE DRAIN/PSUBSTRATE STUDY.

Coefficient	Lens used		
	5X	*20X*	*100X*
β	0.4	0.6	0.7
γ	0.6	0.4	0.3
c_1	2.5	23.8	1000
c_2	55	654	15000

b) *Electrical modeling of the Spatial dependency*

A more complete electrical model, that takes into account the spatial dependency between the induced photocurrent and the laser beam location, is obtained by multiplying equations (1) and (4):

$$I_{ph} = (a \times V + b) \times \alpha_{gauss} \quad (5)$$

3) Wafer thickness effect

The substrate thickness has a significant effect on the photocurrent generation of PN junctions under PLS [8]. The light intensity exponentially decreases throughout the material and so does the photocurrent effect. Indeed more the wafer thickness is thin and more the photocurrent generated on PN junction under PLS was found important.

In order to validate this effect, the photocurrent of a PN junction (Drain/Psubstrate) under PLS on wafers with different thickness was measured. These measures are reported on figure 10. During these experiments, the Drain was biased at 1.2V, the bulk was grounded and the other electrodes were left floating. The laser beam was centered on the drain junction. The laser power was equal to 1.25W. The pulse width of the laser impulsion was set at 20µs.

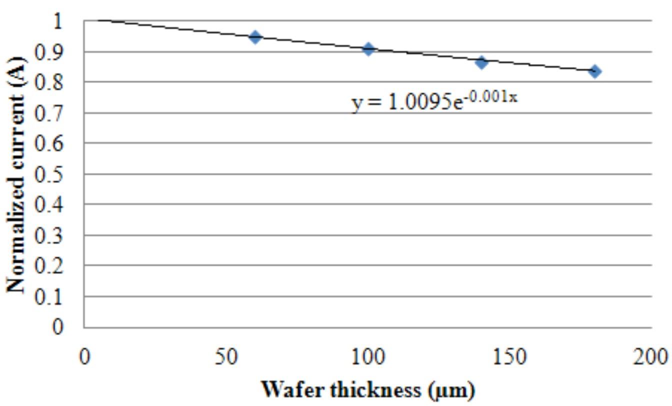


Figure 10. Normalized photocurrent generated in a PN junction versus the wafer thickness.

Therefore it is possible to model the effect of the wafer thickness thanks to equation (6):

$$W_{coef} = e^{-0.001 \times Wafer_{thickness}} \quad (6)$$

where $Wafer_{thickness}$ is the thickness of the wafer expressed in µm. Hence, equation (7), that incorporates the wafer thickness dependency, is obtained by multiplying equations (5) and (6):

$$I_{ph} = (a \times V + b) \times \alpha_{gauss} \times W_{coef} \quad (7)$$

4) Focus effect

Moving the z axis of the laser lens has an influence on the photocurrent generated by a PN junction. In order to highlight the effect of the vertical moving of the z stage of the lens, a Drain/Psubstrate junction of an NMOS transistor (W=10µm / L=10µm) was used and biased as following: the drain voltage was set to 1.2V, the Psubstrate was grounding and the others electrodes were left floating. By convention, when z was equal to 0, the focus was done on the active area of the PN junction. Figure 11 represents the normalized photocurrent induced in the PN junction versus the z axis.

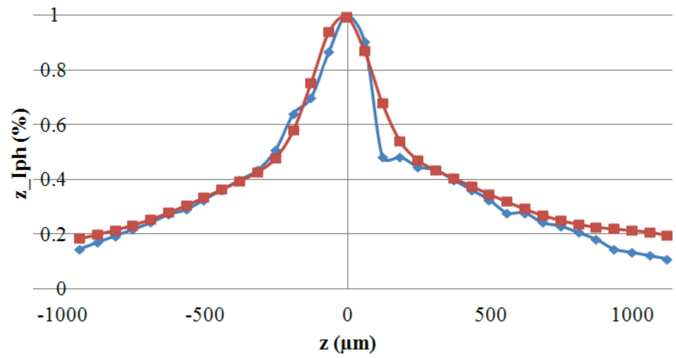


Figure 11. Normalized photocurrent generateg by a PN junction versus the displacement of the axis z of the laser lens which modify the focus.

The model of the *Iph_z* curve is given by equation 8:

$$Iph\_z = (c \times z^6 + d \times z^5 + e \times z^4 + f \times z^3 + g \times z^2 + h \times z + i) \times \left(j \times e^{-\frac{z^2}{20000}} \right) \quad (8)$$

where coefficients *c*, *d*, *e*, *f*, *g*, *h*, *i*, and *j* are expressed in table III.

TABLE III. COEFFICIENTS OF FUNCTION (8) WHICH PERMIT TO APPROXIMATE THE FOCUS EFFECT.

Coefficient	Values
c	-3.E-19
d	-9E-17
e	-8E-13
f	2E-10
g	-8E-7
h	-1E-4
i	0.49
j	0.5

Coefficient *Iph_z*, which takes into account the energy absorption through silicon depending of the wafer thickness, is used to derive the model of equation (9) from equation (8) by multiplication:

$$I_{ph} = (a \times V + b) \times \alpha_{gauss} \times W_{coef} \times Iph\_z \quad (9)$$

Therefore our model of the PN junction under PLS takes into account the position of the laser beam versus the topology of the junction, the wafer thickness, and the focus of the laser beam.

B. NMOS transistor under PLS

1) Study at low laser power

Once the behavior of single PN junctions under PLS is understood and modelled, the phenomena involved when an NMOS transistor is stimulated by a pulsed laser may be studied. In this section an NMOS transistor (W=L=10µm) was used in its OFF state (the drain was at 1.2V and the gate, source and Psubstrate electrodes were grounded). The 20X lens was chosen for this experiment. The pulse duration was set to 20µs, and two different laser powers (25mW and 420mW) were used. At these laser power, we have only observed photoelectrical effects on the NMOS transistor (this was confirmed by TCAD simulations: see figure 12).

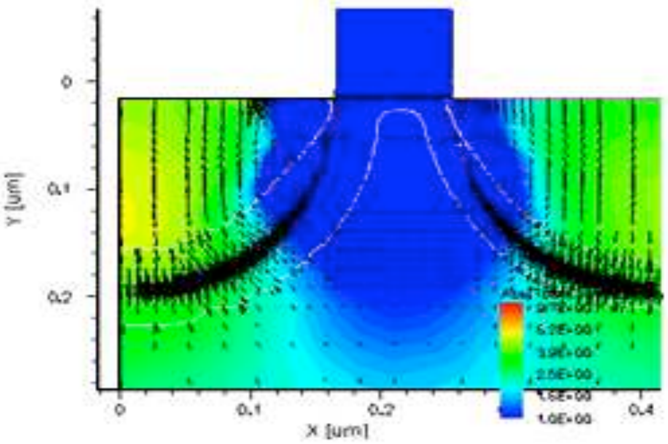


Figure 12. Slide of an NMOS transistor extracted from TCAD simulation which represents the photoelectrical effect induced by PLS.

The photocurrent generated in the two junctions of the transistor has for consequence to increase the local Psubstrate potential.

2) Triggering of the parasitical bipolar NPN (Drain/Psubstrate/Source) at high laser power

a) Measurement correlated with TCAD simulation

A first study of the effect of a locale increase of the NMOS Psubstrate potential was performed without PLS. The bias conditions were set identical to those of the previous measurements. The source, drain and Psubstrate currents were measured versus the Psubstrate voltage which evolved from 0 to 1.2V (see fig. 13).

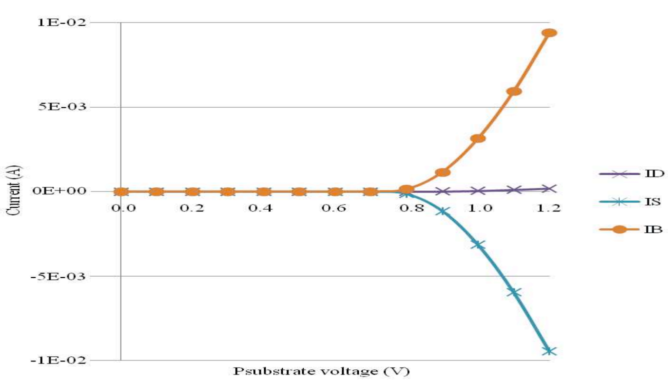


Figure 13. Measured currents of the parasitical bipolar transistor NPN (Drain/Bulk/Source) versus the Psubstrate voltage.

For validation purpose of the measurement results, TCAD simulations without laser stimulation were made. It was also aimed at well characterizing the parasitical bipolar transistor NPN (Drain/Source/Psubstate).

As seen in TCAD simulation, when the Psubstrate voltage is greater than 0.6V, the Psubstrate/Source junction starts conducting. The Psubstrate/Drain junction stays in reverse bias conditions. Therefore an increase of the Psubstrate potential trigs the parasitic bipolar Drain/Psubstrate/Source. The current gain of this bipolar transistor is small (~10^{-3}) since almost the amount of current flows from Psubstrate to source.

b) Electrical model

A specific sub circuit called *Subckt SD* was created in order to simulate the effect of the NPN parasitic bipolar transistor (Drain/Psubstrate/Source). It was built with two voltage controlled current sources (one between Drain and Psubstrate and the other between Psubstrate and source) (See fig. 14). These current sources were calibrated thanks to the measurements reported in figure 13.

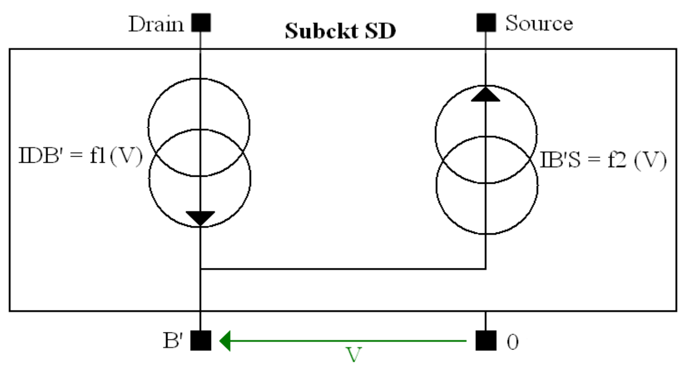


Figure 14. Electrical model of the parasitic bipolar effect under pulsed laser embedded in a sub circuit called Subckt_SD.

C. Model proposed of NMOS transistor under PLS

1) Measurement

Therefore when the laser power is at 1.25W, the local increase of the Psubstrate potential trig the NPN parasitic bipolar (Drain/Psubstrate/Source).

It is also possible to highlight the inversion of the source current during the laser pulse represented by the red arrow. (See fig. 15).

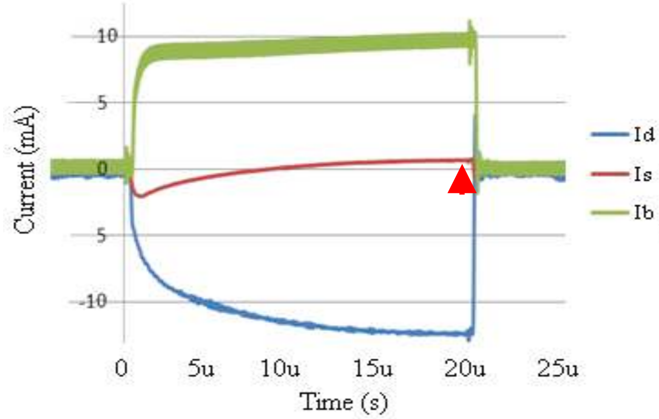


Figure 15. Current measurement of an NMOS transistor under PLS at 1.25W.

2) Electrical model

A proper modeling of the effects of pulsed PLS on an NMOS transistor involved two sub circuits *Subckt_Iph_nplus_psub* (one for the Source/Bulk junction and another for the Drain/Psubstrate junction). It must also involve the effect of a local increase of the Psubstrate's voltage which may trig the parasitic bipolar transistor: *subckt_SD* in figure 16. Resistance Rb and capacitante Cb are used to set the time constant of that phenomenon. This constant describe the time of dielectric relaxation [9].

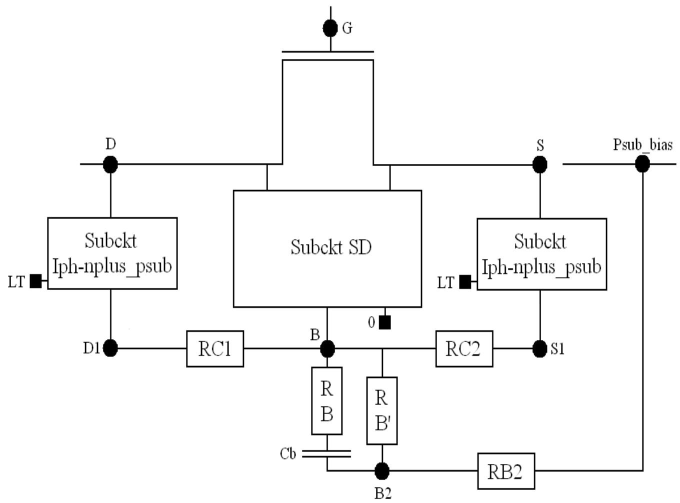


Figure 16. Electrical model of an NMOS transistor under pulsed PLS.

Figure 17 displays the currents simulated for a laser pulse duration of 20µs and a laser power of 1.25W. Note the good correlation obtained between measures (fig. 15) and simulation (fig. 17).

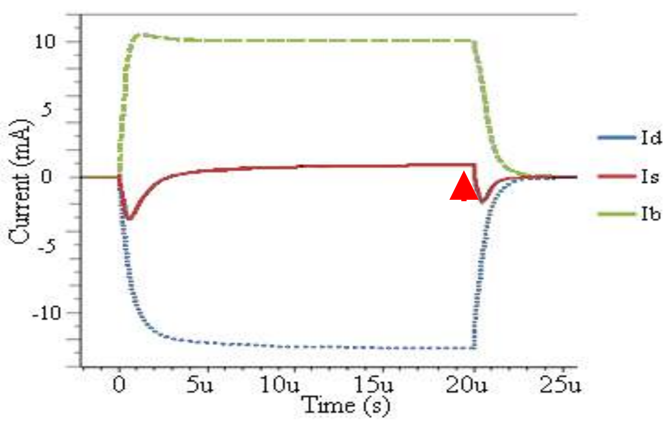


Figure 17. Simulation currents obtained from the electrical model of an NMOS transistor under pulsed PLS.

III. CURRENT CARTOGRAPHIES

A. Principle

The electrical model we have obtained makes it possible to draw current cartographies. It is based on the creation of a mesh on the layout of the transistor. The step of the meshing is a parameter called *stepXY* defined in the ELDO netlist. It is necessary to calculate in every point of the mesh two distances: the distance between the centre of the laser spot and the center of (a) the drain junction, and (b) the source junction.

To illustrate the principle of drawing current cartographies, we have chosen the example of a NMOS transistor (W=L=10µm). The laser power was set near 0W for two main reasons. The first one is that this laser power did not trig the NPN parasitic bipolar transistor Drain/Psubstrate/Source in order to compare the effects of the location of the laser beam on the photocurrent generated on the source and the drain. The second one is that at low laser power the photocurrent generated at the source and the drain is approximately the same whatever the voltage value. Three cases were studied by locating successively the laser spot on the centre of the drain junction, on the centre of the source junction, and in the middle of the NMOS transistor. For each case, drain, source and Psubstrate currents were extracted from the electrical simulation (See Fig. 18).

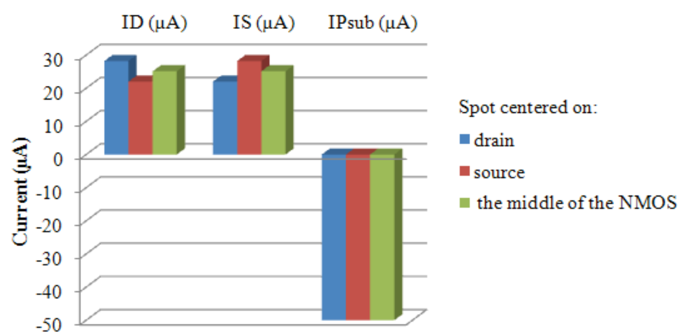


Figure 18. Electrical simulation thanks to ELDO for different localisation of the laser spot.

In a simple case as this one where the meshing is established by only three aligned points, it is possible to define the parameters d_d (distance of the centre of the laser spot to the closest edge of the drain) and d_s (distance of the centre of the laser spot to the closest edge of the source).

$$d_d = m \times stepXY \qquad (10)$$

$$d_s = L - m \times stepXY \qquad (11)$$

In this case *stepXY* is equal to 5µm, with *m* being a parameter evolving between 0 and 2 by step of 1. *L* is the gate length of the NMOS transistor expressed in micrometer.

When the laser beam is centered in the middle of the drain, the photocurrent generated by the drain is more important than the source's photocurrent. The electrical charge conservation of currents is respected. If the beam is centered on the source junction, it is the photocurrent generated by the source that is more important than the drain photocurrent. In the last case, when the laser beam is centered in the middle of the NMOS, the photocurrents generated by the source and the drain are identical (12).

$$I_{PSUB} = 2 \times I_S = 2 \times I_D \qquad (12)$$

On the same principle, it is possible to create more complex cartographies, by creating a denser mesh. The same method is always used. In every point of the mesh, two values of distances are associated. The first value is the distance between the centre of the laser spot and the closest edge of the drain. And the second value is the distance between the centre of the laser spot and the closest edge of the source.

B. Results: Comparison between measurement and simulation

In this section, it is proposed to draw 3D current cartographies (extracted from the ELDO simulator) of photocurrents generated on an NMOS transistor W=L=10µm and to compare it with measurements. The laser power was maximal (1.25W). It is also possible to extract 3D cartographies of photocurrents generated by the two PN junctions of an NMOS [10].

Figures 19a and 19b highlight the good correlation between electrical simulation and measurements.

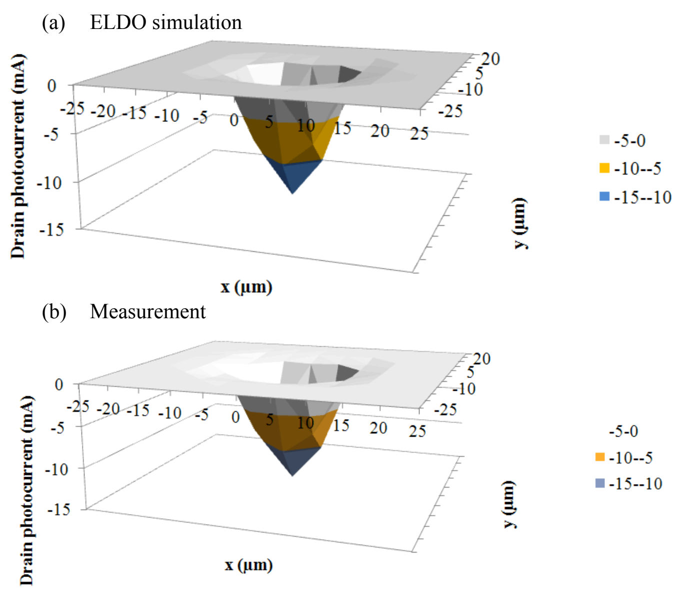
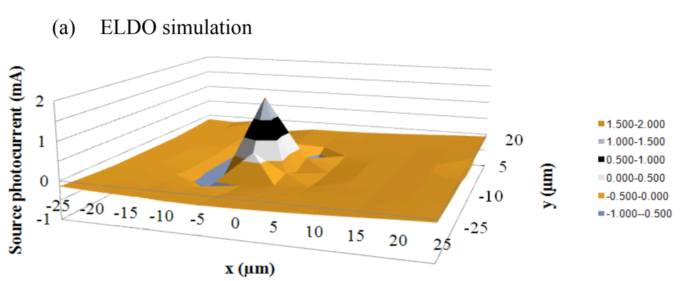


Figure 19. 3D current cartographies of the photoelectrical contribution of the drain under PLS extracted from ELDO (a) and measurement (b).

It is also possible to extract cartographies of the source current (electrical simulation and measurements are respectively reported in fig. 20 (a) and (b)).



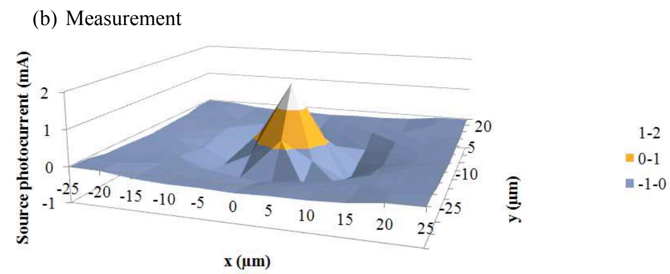


Figure 20. 3D current cartographies of the photoelectrical contribution of the source under PLS extracted from ELDO (a) and measurement (b).

Source cartographies highlight the triggering of the NPN parasitic bipolar transistor (Drain/Psubstrate/Source). This phenomenon appears when the laser beam is centered on the transistor (The current value is positive).

The same process than for source and drain current cartographies was made for the Psubstrate. (See fig. 21a and 21b).

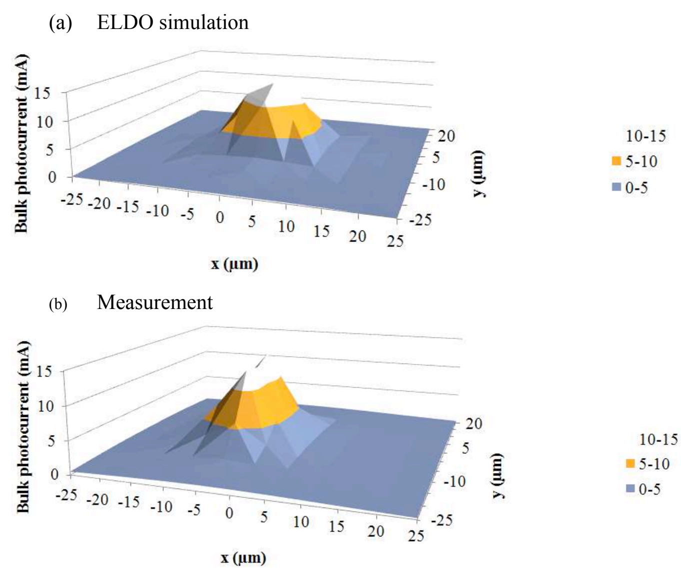


Figure 21. 3D current cartographies of the photoelectrical contribution of the bulk under PLS extracted from ELDO (a) and measurement (b).

IV. Conclusion

The process of building an accurate electrical model of an NMOS transistor in 90nm technology under pulsed laser was reported in this paper. The phenomena revealed by measurement were included in our model (i.e. the triggering of the parasitic bipolar transistor beyond a laser power of ~1W). The validity of the approach was assessed by the very good correlation obtained between electrical simulations (based on SPICE language) and measurements. TCAD physical simulations were also ran to explore the underlying physical phenomena. In failure analysis it could have a great utility in order to compare the simulated response of a golden circuit under pulsed laser with actual measurements. This work will be extended to PMOS transistors which contains an additional

Nwell/Psubstrate junction. Due to this fact, the model will be more complex, with three PNP parasitic bipolar transistors (One Source/Nwell/Drain, anothers Drain/Nwell/Psubstrate and Source/Nwell/Psubstrate). Therefore, as a perspective, it will permit us to simulate the behavior under pulsed laser of complex logic gates made of NMOS and PMOS transistors.

REFERENCES

[1] ELDO user's Manual – Software Version 6.6_1 Release 2005.3- Mentor Graphics user's manual, 2005.

[2] R. Minixhofer, "TCAD as an integral part of the semiconductor manufacturing environment", Simulation of Semiconductor Processes and Devices, vol. issue pp. 9-16, 2006.

[3] A. Glowacki, ph. D Thesis, 2010, Berlin University of Technology ― Expanding the scope of laser stimulation techniques for functional analysis and reliability of semiconductor devices by in-depth investigation of the optical interaction with the devices.

[4] Characterization and TCAD simulation of a 90nm technology NMOS transistors under continuous photoelectric laser stimulation for failure analysis improvement, R. Liddo, A. Sarafianos, O. Gagliano, V. Serradeil, V. Goubier, M. Lisart, J-M Dutertre, A. Tria, V. Pouget, D. Lewis, IPFA 2012.

[5] Characterization and TCAD simulation of a 90nm technology PMOS transistors under continuous photoelectric laser stimulation for failure analysis improvement, R. Liddo, A. Sarafianos, O. Gagliano, V. Serradeil, V. Goubier, M. Lisart, J-M Dutertre, A. Tria, V. Pouget, D. Lewis, ISTFA 2012.

[6] Building the electrical model of the Photoelectric Laser Stimulation of an NMOS transistor in 90nm technology. A. Sarafianos, R. Llido, O. Gagliano, J-M Dutertre, V.Serradeil, M. Lisart, V. Goubier, A. Tria, V. Pouget, D. Lewis, ISTFA 2012.

[7] Building the electrical model of the Photoelectric Laser Stimulation of an PMOS transistor in 90nm technology. A. Sarafianos, R. Llido, O. Gagliano, V.Serradeil, M. Lisart, V. Goubier, J-M Dutertre, A. Tria, V. Pouget, D. Lewis, ESREF 2012.

[8] V. Pouget, ph. D Thesis, Université Bordeaux I, 2000, Simulation expérimentale par impulsions laser ultra-courtes des effets des radiations ionisantes sur les circuits intégrés.

[9] A. Douin, ph. D Thesis, Université Bordeaux I, 2008, Contribution à la modélisation et au développement de techniques de test et d'analyse dynamique de circuits intégrés par faisceau laser pulsé.

[10] A. Glowacki, S. K. Brahama, H. Suzuki, C. Boit. ―Systematic characterization of integrated circuit standard components as stimulated by scanning laser beam, ISTFA 2010.