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Abstract— **This paper presents the design of an SRAM cell with a robustness improvement against laser-induced fault injection. We report the fault sensitivity mapping of a first SRAM design. A careful analysis of its results combined with the use of an electrical model at transistor level of the photoelectric effect induced by a laser permit us to validate our approach. The robustness improvement is due to a specific layout which takes into account the topology of the cell and to the effect of a triple well implant on the laser sensitivity of NMOS transistors.**

Keywords-component; SEU; SRAM cell; pulsed PLS; 1064nm wavelength; electrical simulation, robusteness

I. INTRODUCTION

SRAM memory cells are prone to Single Event Upset (SEU) when exposed to ionizing particle hits (in harsh a radioactive environment). An SEU consists in an inversion of the data bit stored by the struck SRAM. SEU were strongly take into account when further problems were observed in space electronics devices during the 1960s due to the high exposition of chips embedded in space vehicles to radioactive particles emitted mainly by the sun. Nowadays, SEU is yet a major threat for semiconductor manufacturers. The robustness of chips against SEU could be tested by a cyclotron or pulsed laser equipment using the Photoelectrical Laser Stimulation (PLS) effect induced in silicon. However this kind of experiments could be very expensive and time consuming. Physical (i.e. TCAD) simulation [1, 2] may be used, but a Spice simulation is faster [3]. In this context, it is interesting to use a simulation tool at gate level in order to simulate with good accuracy the effect of PLS on a chip in order to analyze its sensitivity to SEU in a very small amount of calculation time. In this paper, we present an electrical model of the backside PLS of an SRAM cell in 0.25 µm CMOS technology. We used a pulsed laser at 1064 nm wavelength to conduct the PLS experiments. The obtained measurements were used to build an electrical model of the cell under PLS and to analyze its behavior. This electrical model makes it possible to simulate the response of the SRAM cell to laser pulses in a very small amount of calculation time.

Moreover, comparisons between simulations and measurements will rather be qualitative than quantitative due to the fact that the electrical model of PN junctions under PLS was tuned thanks to measurements on a STMicroelectronics 90 nm technology.

Electrical models of PN junctions under pulsed laser stimulation (N+ on Psubstrate, P+ on Nwell and Nwell on Psubstrate) were previously introduced [4, 5]. We have also already introduced electrical models, based on preliminary studies made from measurements and TCAD simulations [6, 7] for continuous PLS at low laser power (under ~100 mW), which create only photoelectrical effects [8, 9]. This model consists in a simple current source controlled by voltage to model the laser induced photocurrent. The novelty of the model presented in this paper is that it is the first model of a relatively complex CMOS cell made from NMOS and PMOS transistors under pulsed PLS which takes into account the topology of the target (i.e. the layout of the cell) relatively to the effect area of the laser beam which have a *Gaussian-like* intensity profile.

This paper is organized as follows. Section II presents, from a theoretical point of view, the SEU sensitivity of an SRAM cell exposed to PLS. In theory four sensitive areas are expected. Section III reports measurements on an actual SRAM cell. It turns out that only three sensitive areas were revealed: a masking effect of the forth sensitive area appeared. The Gaussian intensity profile of the laser beam and the topology of the cell could explain this unexpected result. Moreover, electrical modeling and related simulations confirm this particular result. Sensitivity maps obtained from simulations and measurements showed a very good correlation. This validates the relevance of our simulation tool. In section IV, a new solution to increase the SEU robustness of a standard six transistors (6T) SRAM cell is introduced. This new design involved the use a triple well (deep Nwell) implant under the NMOS transistors of the SRAM cell and a careful positioning of the cell's transistors. The latter technique takes advantage of the SEU sensitive area masking effect analyzed in section 3. The new 6T SRAM cell was then tested with our electrical model. Finally, our findings are summarized in the concluding section V with some perspectives.

II. EFECT OF SINGLE EVENT UPSET ON AN SRAM CELL

The photoelectric effect is generated by a laser beam passing through silicon provided that its photons energy is greater than the silicon band gap [10]. This effect creates electron-hole pairs along the laser path. Generally these pairs recombine and there is no noticeable effect on the IC's behavior. However, under specific conditions, some undesired effects may appear: the so-called Single Event Effects (SEE).

A SEE happens when the charge carriers (i.e. electrons and holes) created by the laser beam are drifted in opposite directions by the electrical field found in the PN-junctions of CMOS transistors instead of recombining. As a consequence a transient current (i.e. moving charge carriers) is generated through the struck junction. After the creation of the electron-hole pairs along the laser beam, two phenomena lead to the creation of the transient current: the prompt charge collection, or funneling, and the diffusion. The first phenomenon stretches the depletion region (where it exists a strong electric field) along the laser beam, within a few picoseconds the charges nearby are collected giving a current peak. Then, in a second time, the remaining charges are collected in a longer diffusing scheme: the diffusion [11]. When such a transient current is induced in the logic of a memory cell it may cause the flipping of its logical state: a so-called SEU.

A. *Description of the studied SRAM cell*

The cell studied in this section of the paper is a configuration SRAM (CSRAM) made of five transistors (see fig. 1) similar to those used to store the configuration bitstream in programmable devices (FPGA). The SRAM is embedded in a test chip designed in a CMOS 0.25 µm process. However, we will rather use the term SRAM in this paper, since its main results may be generalized to 6 transistors SRAM cells.

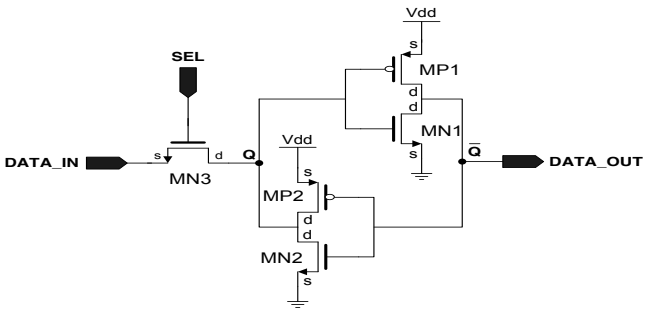

Figure 1. Schematic of the CSRAM cell.

When the selection signal (*SEL*) is at a high state (*SEL="1"*) the SRAM cell is in write mode: *DATA_IN* is applied to node *Q* through transistor *MN3*. This value is then latched by the two coupled inverters made from *MP1*, *MN1*, *MP2* and *MN2*. In the following the sensitivity of the cell to PLS is studied according the SRAM cell schematic and its bias conditions. A sensitive node of a CMOS gate is defined as a node in a circuit whose electrical potential can be modified by internal injection or collection of electrical charges.

B. *Study of the SEU sensitivity of the SRAM cell*

In this subsection, the SRAM SEU sensitivity is studied from a theoretical point of view (considering its schematic and its state) in its hold state (i.e. its access transistor *MN3* is OFF).We refer to state one (respectively state zero) when the node *DATA_OUT* is in high state (resp. low state). The sensitivity of the cell can be investigated by considering which PN junctions are the most reverse biased in function of the SRAM state. Indeed, these reverse biased PN junctions are the place where the electrical field is strong enough to generate a transient current likely to induce an SEU. Two cases are considered: states "1" and "0". The red arrows in figures 2 and 3 also give the directions of the induced photocurrents between the transistors drain and bulk or source and bulk. The thick arrows represent strong photocurrents, the thin arrows smaller ones.

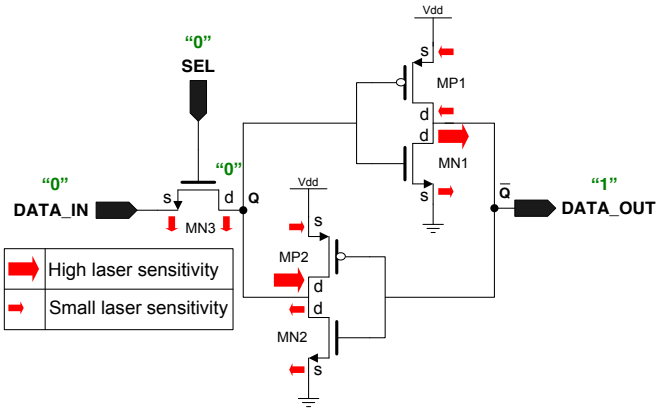

Figure 2. Schematic of the SRAM cell laser sensitivity in state "1".

In state "1", depicted in fig. 2, the two most sensitive areas to laser illumination are the drain junctions of *MN1* and *MP2*. In state "0", depicted in fig. 3, the intensities of the induced photocurrents are inverted in comparison with the state "1": the two most sensitive areas are the drains of *MP1* and *MN2*/*MN3* (note that *MN2* and *MN3* share a common drain diffusion, see the SRAM's layout in fig. 5). Therefore four sensitive areas are expected: two in state "0" and two others in state "1".

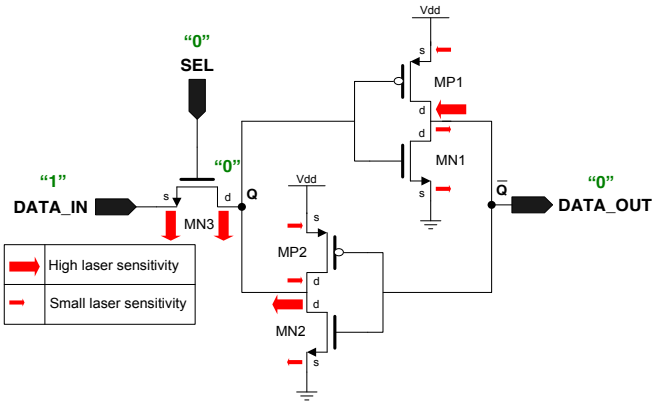

Figure 3. Schematic of the SRAM cell laser sensitivity in state "0".

III. MEASUREMENT AND ELECTRICAL MODDELING OF THE SEU SENSITIVITY OF AN SRAM CELL

A. *Measurement*

The SRAM test series were performed with a pulsed laser equipment (at 1064 nm wavelength, 0.16 µJ energy, and 50 ns pulse duration). The laser beam's spot diameter was set to 1 µm. Injection experiments were performed by exposing the front side of the SRAM cell. This cell was designed with a minimum of metallization, in order to be able to perform front side and backside laser injection. The absorption of the silicon at 1064 nm wavelength is weak. The carriers are also deeply created and can drift quite for approximately 10 or more µm. These two phenomena have probably as effect to increase the surface of the sensitive areas in comparison with cosmic rays, which are more point sources in comparison with the diameter of our laser spot. However, the SEU sensitivity mapping we have obtained in these conditions is drawn in figure 4. Dark red color is used to depict SEU sensitivity in state "0", and blue color to depict SEU sensitivity in state "1". As the laser spot is targeting a red case on this map and provided the SRAM is in state "0" an SEU occurs: the cell flips to state "1". Respectively, as the laser spot is targeting a blue case on this map and provided the SRAM is in state "1" an SEU occurs too: the cell flips to state "0".

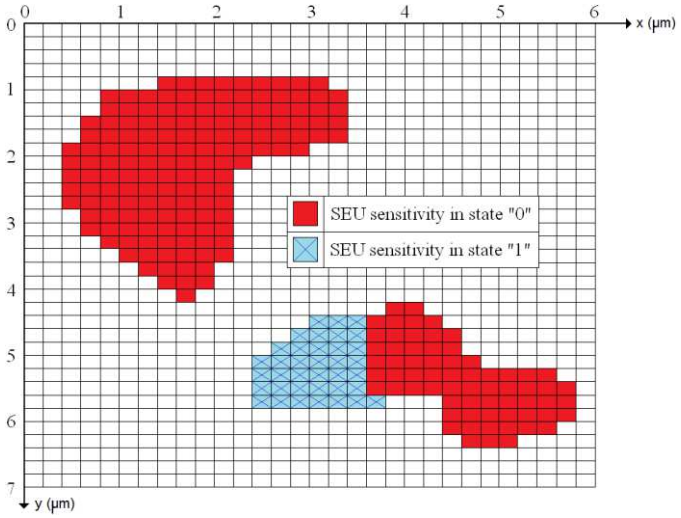

Figure 4. Experimental SEU sensitivity map of the SRAM cell at a laser energy equal to 0.16 µJ.

Only three sensitive areas were experimentally revealed (see fig. 4), despite four were theoritically expected. An explanation of the discrepancy between theory and experiment lies in the fact that the previous theoritical analysis was made according the assumption that a laser shot only affect one sensitive area. However, this assumption does not hold experimentally because PLS may induce photocurrents in several PN junctions depending on the target's topology and on the location and size of the laser spot. Indeed, the laser beam's effect area has a Gaussian like profile and its effect may extend beyond the spot size.

Moreover, the trend in continuously reducing the technology size makes it very difficult to illuminate only one junction without creating effects on the others. This is the reason why it is needed to take into account the topology and size of the cell and the effect of the laser on several junctions at the same time. The layout of the studied SRAM cell is depicted on figure 5. Its size is 4x9 µm. Note that transistors *MN2* and *MN3* have a shared drain diffusion (which is close to the drain of *MP2*).

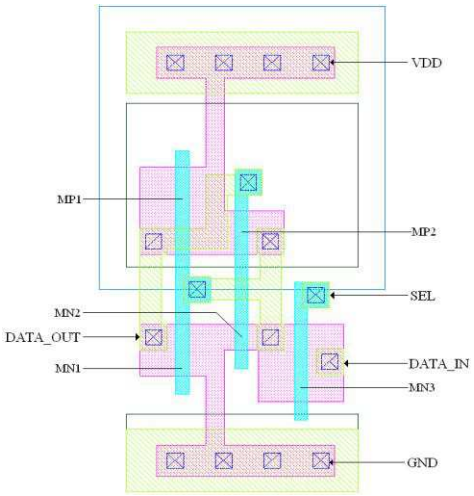

Figure 5. Layout of the SRAM cell.

We made the hypothesis that this layout has the effect to mask the sensitivity of *MP2*'s drain (which is the missing sensitivity area in fig. 4). Figure 6 illustrates this masking effect which originates from the photocurrent generated by the drain shared between *MN2* and *MN3* (blue arrows) that counterbalances the effect of the photocurrent induced in the Drain/Nwell junction of *MP2* (crossed arrow). This effect lies in the proximity between the drains of *MP2* and *MN2*/*MN3*, and also in their sizing.

Therefore with a topological approach there is only one sensitive area in state "1" which is the drain/Psubstrate junction of *MN1*. There is no such similar counterbalancing effect in state "0".

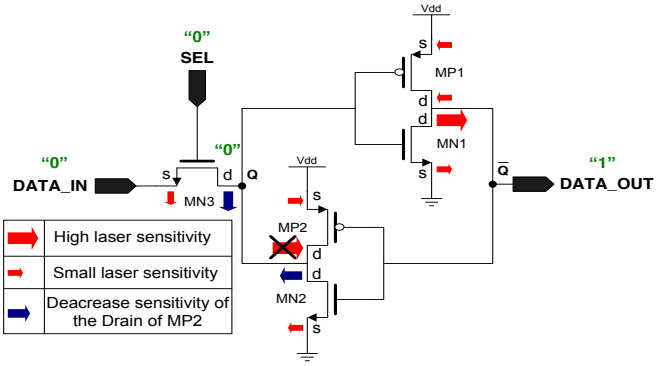

Figure 6. Schematic of the SRAM cell laser sensitivity in state "1", with a layout approach.

It is then proposed to illustrate thanks to electrical modeling the effect of the cell's topology which gives only three sensitive areas, while four are expected in theory.

B. Electrical modeling

In this section we present an electrical model of the SRAM cell under Photoelectrical Laser Stimulation. In this model we consider that the laser power used in measurement and electrical simulations are not capable to trig the different parasitical bipolar transistors present in this cell [12].

For every PN junction, a sub circuit which contains a specific controlled voltage current source is added to the netlist of the SRAM cell (See Fig. 7) to model the laser-induced photocurrents. These models were built and validated from actual measurements on transistors. This research work is reported in [5, 6].

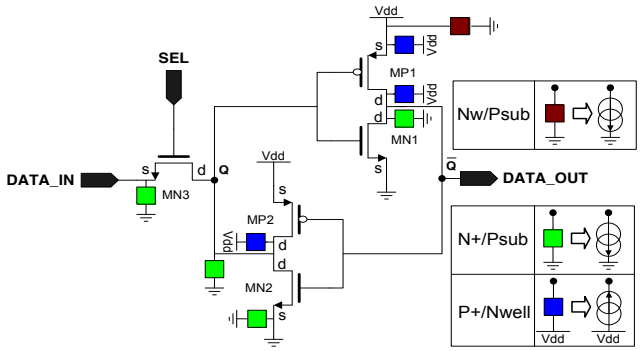

Figure 7. Electrical model of the SRAM cell under PLS.

The current amplitude of the current source of each PN junction is defined thanks to equations presented on Table I.

TABLE I. EQUATIONS WITH COEFFICIENTS WHICH CONTROL THE PHOTOCURRENT GENERATED BY THE PN JUNCTIONS OF THE SRAM CELL DURING THE LASER PULSE.

$$I_{ph} = (a \times V + b) \times S \times \alpha_{gauss} \times V_{laser\_trig}$$

$$a = p \times P_{laser}^{\ 2} + q \times P_{laser} + r \qquad b = s \times P_{laser}$$

Coefficient	N+/Psub	P+/Nwell	Nwell/Psub
p	$4E^{-9}$	$9E^{-5}$	$6E^{-11}$
q	$-5E^{-7}$	$2E^{-4}$	$9E^{-9}$
r	$9E^{-6}$	$-5E^{-6}$	$1E^{-7}$
s	$4E^{-6}$	$1.2E^{-3}$	$6E^{-8}$

$$\alpha_{gauss}(d) = \left[\beta \times \exp\left(-\frac{d^2}{c_1} \right) + \gamma \times \exp\left(-\frac{d^2}{c_2} \right) \right] \times w$$

I_{ph} is the photocurrent generated during the laser pulse expressed in Ampere. P_{laser} is the laser power expressed in Watt. The function α_{gauss} expressed in % is a function which defines the spatial dependency of the photocurrent (d is the distance, expressed in µm, between the laser spot and the PN junction of interest).

In this layout there are some junctions which are shared (sources of *MP1* and *MP2*, sources of *MN1* and *MN2*, and drains of *MN2* and *MN3*). It is the reason why only eight sub circuits are connected to the SRAM netlist. Results obtained in electrical simulations are more qualitative than quantitative. Indeed, our electrical modeling could reveal the number of sensitive areas ant a trend of their surfaces.

C. Measurement versus electrical simulation

In this section, cartographies made from our electrical model are presented. We used a 0.5 µm step to draw the SEU sensitivity map depicted in figure 8. The simulator was used in order to take into account the topology of the target relatively to the location of the laser beam. SEU sensitivity in state "0" is drawn in red, whereas SEU sensitivity in state "1" is drawn in blue. These simulation results are well correlated to the measurement results (cf. figure 4): the sensitivity of *MP2*'s drain in state "1" is masked. This provides a high confidence in the validity of our modeling of PLS at transistor level and of its use to perform SEU sensitivity studies. The next section reports the use of this methodology to analyze and improve the SEU sensitivity of a 6T SRAM cell.

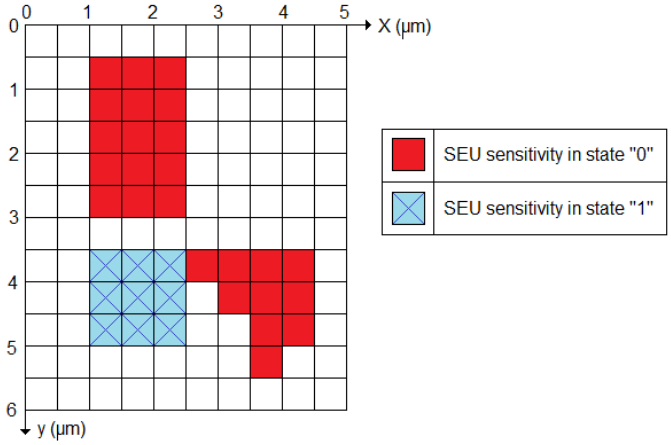

Figure 8. Simulation-based SEU cartography of the SRAM cell.

IV. SRAM ROBUSTNESS IMPROVEMENT

The first part of this section describes attempts to decrease the number of sensitive areas by using the previously described masking effect. The second part reports the use of triple well (deep Nwell) implant [15] to obtain a further decrease of SEU sensitivity. The study was done now on a standard 6T SRAM cell designed in CMOS 90 nm technology.

A. Decreasing the number of SEU sensitive areas

The schematic of the 6T SRAM cell is presented in fig. 9.

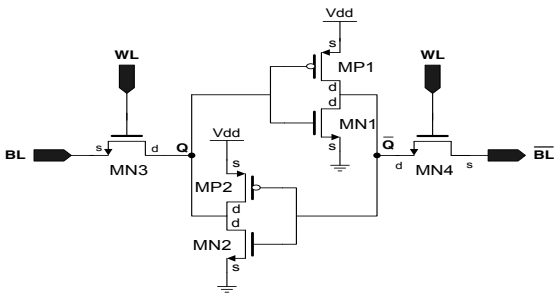

Figure 9. Schematic of the standard 6T SRAM cell.

In state "0" (defined for Q in low state), a masking effect of *MP2*'s SEU sensitivity (similar to that described in the previous section) may be obtained by placing the shared drain of the NMOS transistors *MN2* and *MN3* in its closeness. Likewise, in state "1" (defined for Q in high state), the SEU sensitivity of *MP1*'s drain may be masked by placing the shared drain of *MN1* and *MN4* close to it. The previous placing constraints were used to draw the layout of the 6T SRAM cell as depicted in figure 10 (we have also followed the guidelines given in [14] for the drawing of SRAM layout).

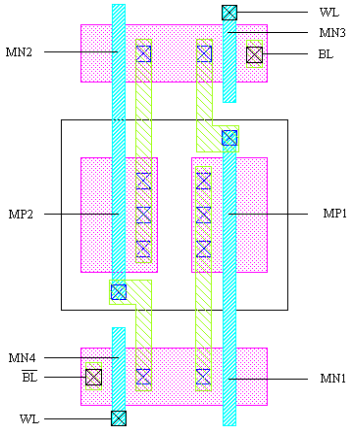

Figure 10. New layout of the more robust SRAM cell.

The corresponding SEU sensitivity map drawn from electrical modeling of PLS and simulation is given in figure 11.

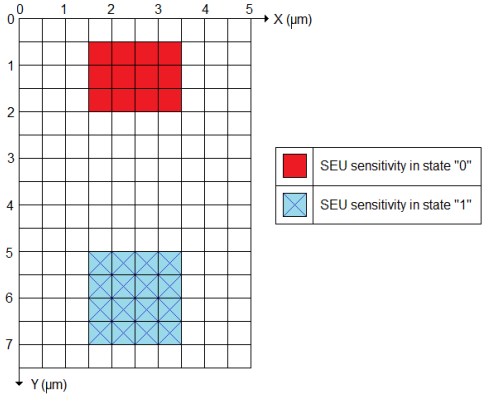

Figure 11. SEU sensitivity map of the 6T SRAM cell.

This layout solution of the 6T SRAM cell has removed the two sensitive areas of *MP1* and *MP2* (one more than for the 5T SRAM cell thank to the additional access transistor *MN4*). However there are always two remaining sensitive areas which are the shared drains of NMOS transistors *MN1*/*MN4* and *MN2*/*MN3*. In the following a solution is proposed to decrease the threshold of these sensitive areas.

B. SRAM cell using triple well implant

1) Triple well effect on NMOS transistor

a) Measurement

Another approach in order to increase the robustness of the SRAM cell under PLS is to use triple well implant (i.e. a deep Nwell implant) under NMOS transistors. This implant modifies strongly the collection charge mechanism which occurs on an NMOS transistor. In these conditions the most important photocurrents are generated by the deep Nwell/Psubstrate and the deep Nwell/Pwell junctions, which have for effect to decrease the photocurrent generated by the two N+/Pwell junctions. Moreover, but in small proportion, this implant creates an optical interface between the deep Nwell and the Psubstrate: a reflection phenomenon takes place. As a result, due to these two effects, the induced photocurrents at the NMOS transistors' N+/Pwell junctions should be reduced. In order to study the influence of the deep Nwell implant on an NMOS transistor we have compared the photocurrents generated on an NMOS transistor, in OFF state, with and without deep Nwell. The biasing conditions of the NMOS deep Nwell transistors are the followings: the source, the gate and the triple well are biased at 1.2V, and the Psubstrate, the Pwell and the drain are grounded.

Figure 12 presents the photocurrent measured on NMOS transistors with and without a deep Nwell implant.

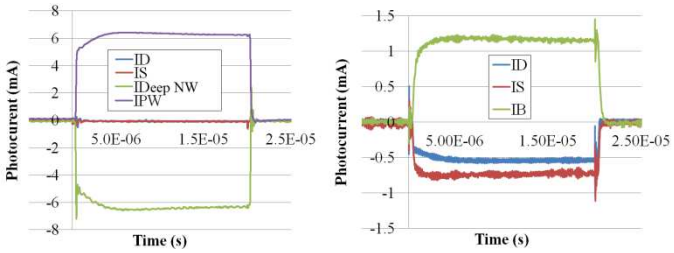

Figure 12. Photocurrent generated on an NMOS transistor with (left) and without deep Nwell (right).

The photocurrents measured on the drain (ID) and the source (IS) of the NMOS transistor with deep Nwell are negligeable in comparison with the photocurrents generated by the deep Nwell/Psubstrate junction (IPW and IDeep Nw). This result is confirmed by TCAD simulations. The triple well implant (which also creates a strong photocurent generation between the deep Nwell and the Psubstrate) leads to a decrease by a factor of 10 of the photocurrent induced in and pushed through the drain of the NMOS. The latter photocurrent is the one that may cause a SEU.

b) TCAD simulation

In order to confirm the trend seen in measurement, TCAD simulations were ran. Two TCAD structures were built: a standard NMOS transistor (fig. 13a), and a NMOS with deep Nwell transistor (fig 13b).

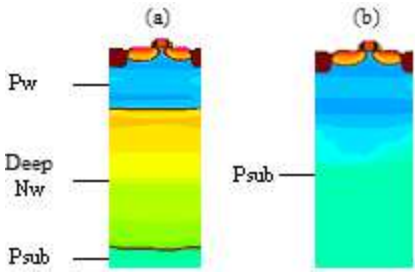

Figure 13. TCAD cuts with (a) and without deep Nwell implant (b).

Results of the photocurrent generation between an N+/Psubstrate junction and an N+/Pwell junction are presented in table II. As seen in measurement, the deep Nwell implant decreases the photocurrent generation on the drain of the NMOS transistor.

TABLE II. COMPARISON OF THE PHOTOCURRENT GENERATION BETWEEN AN NMOS TRANSISTORI WITH AND WITHOUT DEEP NWELL.

	IDNMOS (A)	IPsub (A)
STD	3.1E-12	1.08E-10
deep Nwell	1.1E-12	3.33E-9

2) New layout proposal of the 6T SRAM cell using triple well implant

A triple well (deep Nwell) was added to the layout depicted in figure 10. The same kind of electrical simulation for the purpose of drawing its SEU sensitivity cartography was then ran. The model we used took into account the effect of the triple well on PLS (the model was tuned thanks to the actual measurements reported previously).

At the same simulated laser power which was used in order to draw the electrical cartography presented in figure 11, all the sensitive areas of the cell have disappeared. An increase by a factor of 4 of the simulated laser power is needed to make it reappear.

V. CONCLUSION

An analysis of the laser induced sensitive nodes of an SRAM cell was firstly reported in this paper. The preliminary conclusion of this theoretical analyze was that there are two sensitive areas of the SRAM cell which modify the output from “0” to “1” and two others for an output state modification from “1” to “0”. However this conclusion was not verified in practice. The topology of the cell has a strong impact on the sensitivity of a CMOS gate. A masking effect occurred: only one area which modifies the output node from “1” to “0” was revealed. This phenomenon revealed by measurement cartographies was also confirmed by proper electrical simulations that take into account the topology of the target and the induction of photocurrents in several sensitive nodes. The validity of the approach was assessed by the very good correlation obtained between electrical simulations (based on SPICE language) and measurements. This model permits us to propose and to validate (on simulation basis) a new layout of a standard 6T SRAM cell more robust against SEU. The SEU robustness of PMOS transistors is obtained thanks to the masking effect provided by the photocurrents induced in the NMOS’ sensitive junctions. We also used a deep Nwell implant to increase the SEU robustness of the SRAM’s NMOS. As a result the SEU sensitivity threshold of the SRAM was significantly raised. The main interest in increasing the robustness of CMOS gates is that it will be necessary to increase the laser power in order to obtain the same effects. This laser power increase could be more easily detected by SEU sensors which could be embedded on a chip [15]. Moreover, this sensitivity improvement of the cell could permit to decrease the number of these sensors on the die too. As a conclusion we can say that the electrical model presented in this paper could be an interesting tool for designer who wants to build more robust CMOS gates against SEU effects or against fault injection in the security field.

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