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Discussion on the Model of Laser Induced Faults in SRAM Memory cells

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- Faults are often modeled according two fault models:
 - Bit Set (resp. Reset)
 - Bit Flip
- Not much analysis on the fault model in SRAM:
 - Faults type
 - Effects of the fault injection on the SRAM

➔ Analyze the fault model on SRAM memory cell



- Introduction
 - Fault model
 - Fault injection mechanism
 - Sensitivity zones
- Experiments on the SRAM cell
 - Description of the SRAM memory cell
 - Sensitivity map
- Spice Simulation
 - Sensitivity map
 - Simulation on the edge zone
- Conclusion & Perspectives



Bit set(resp. reset)

- Its value is changed: '0' => '1'(resp. '1'=>'0')
- Result in a calculation error
- Unfaulted if its value was already '1'(resp. '0')
- **Allow to mount safe error attacks**

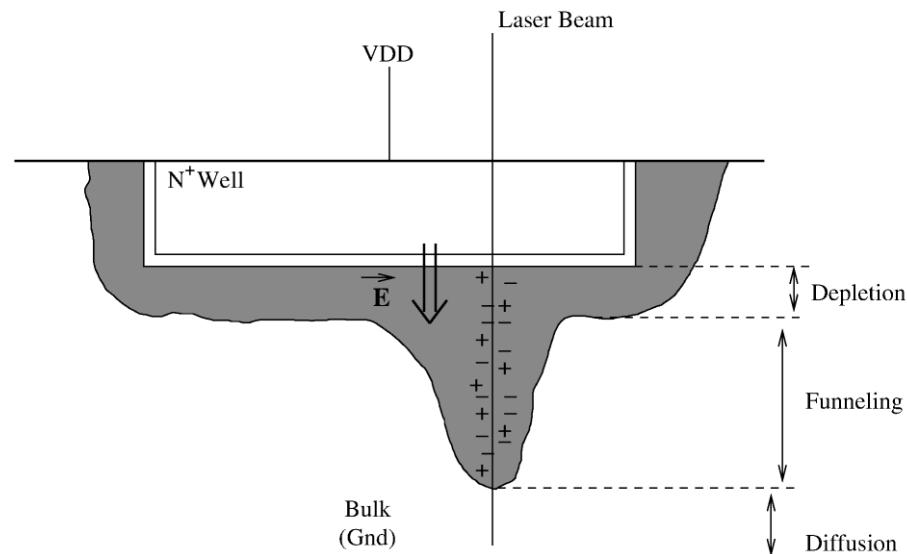
Bit flip

- Independent of the data value ('0' => '1 or '1' => '0')
- Induces a calculation error
- Better fault injection rate
- Quicker analysis of the faulted results



Fault injection mechanism

- Creation of electron-hole pair along the laser beam due to the photoelectric effect
- Stretch the electric field
- Creation of a transient current
- Possible SEE on PN junction
 - Source and drain of transistors

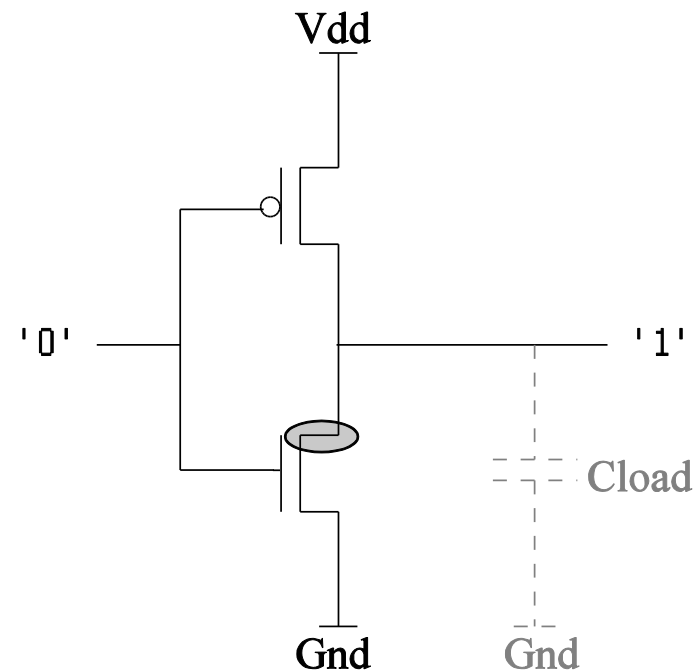




Sensitivity zones

- Inverter's case:
 - 1st Case (output = '1')
 - PMOS ON
 - NMOS OFF
 - Only a strike on drain of NMOS will discharge the load and change the output state

The sensitivity zone is the drain of the OFF NMOS transistors

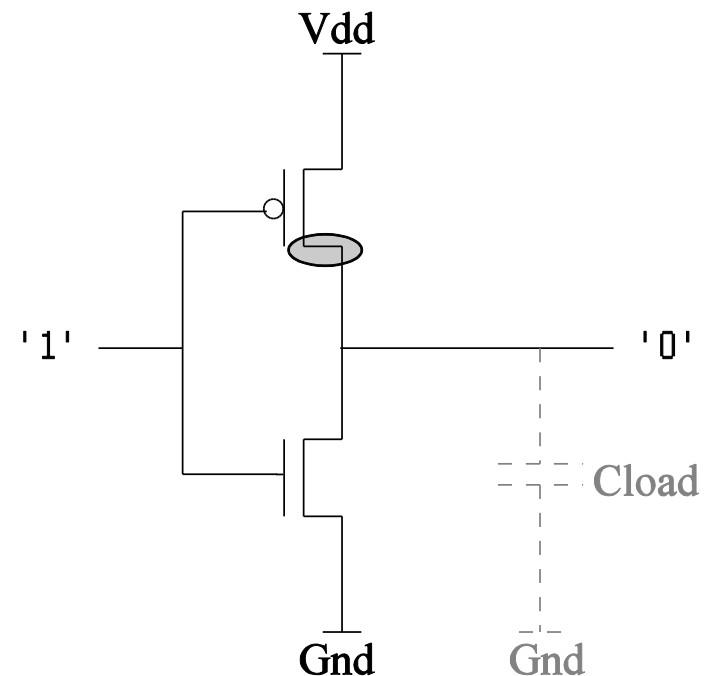




Sensitivity zones

- Inverter's case:
 - 2st Case (output = '0')
 - PMOS OFF
 - NMOS ON
 - Only a strike on drain of PMOS will charge the load and change the output state

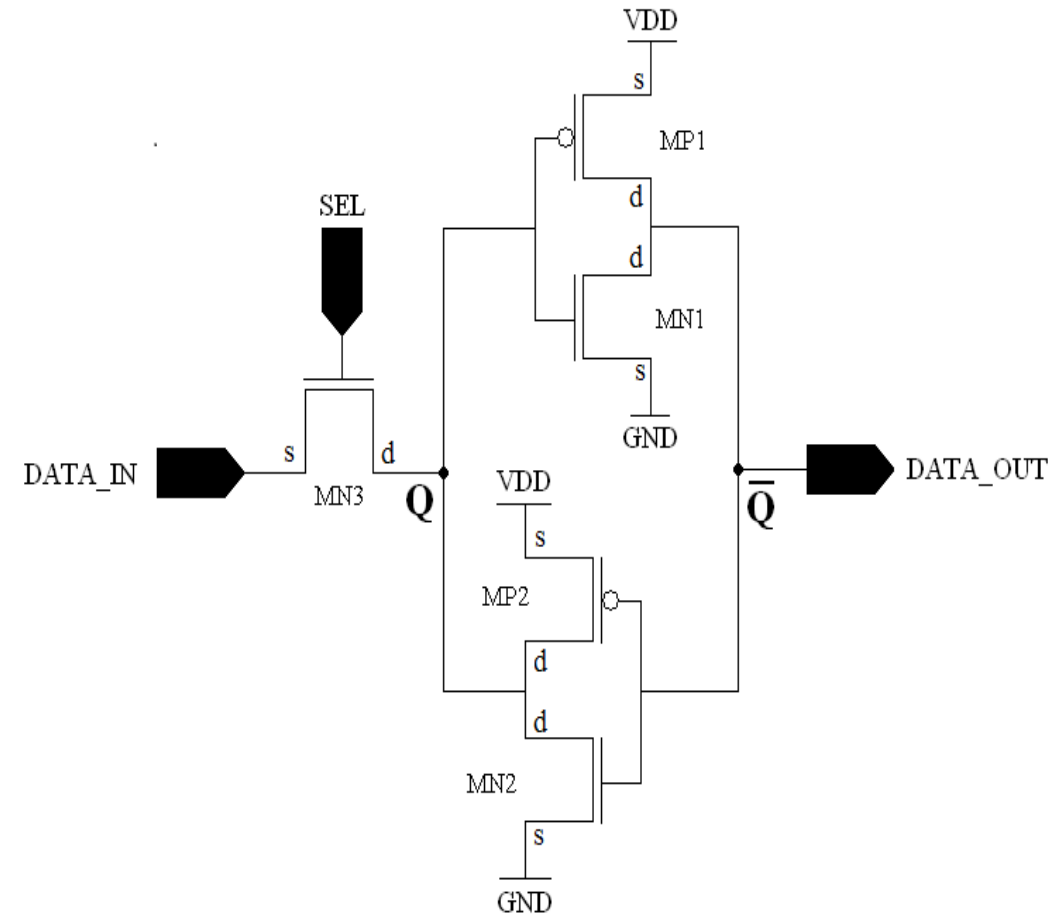
The sensitivity zone is the drain of the OFF PMOS transistors



SRAM Memory Cell



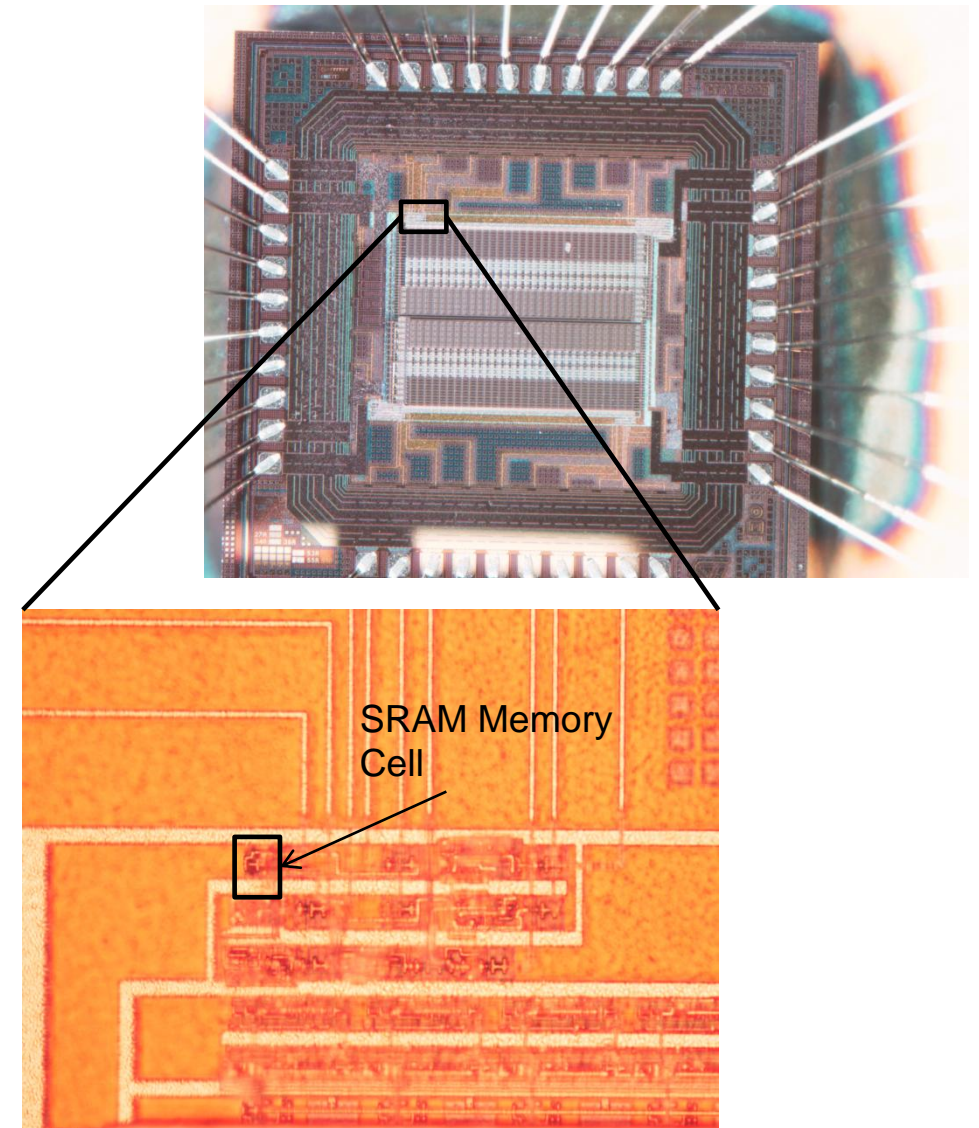
- Configuration SRAM (programmable logic)
 - 5 transistors
- 0.25 μm CMOS Technology
- Size: 9 μm x 4 μm





Experimental setup

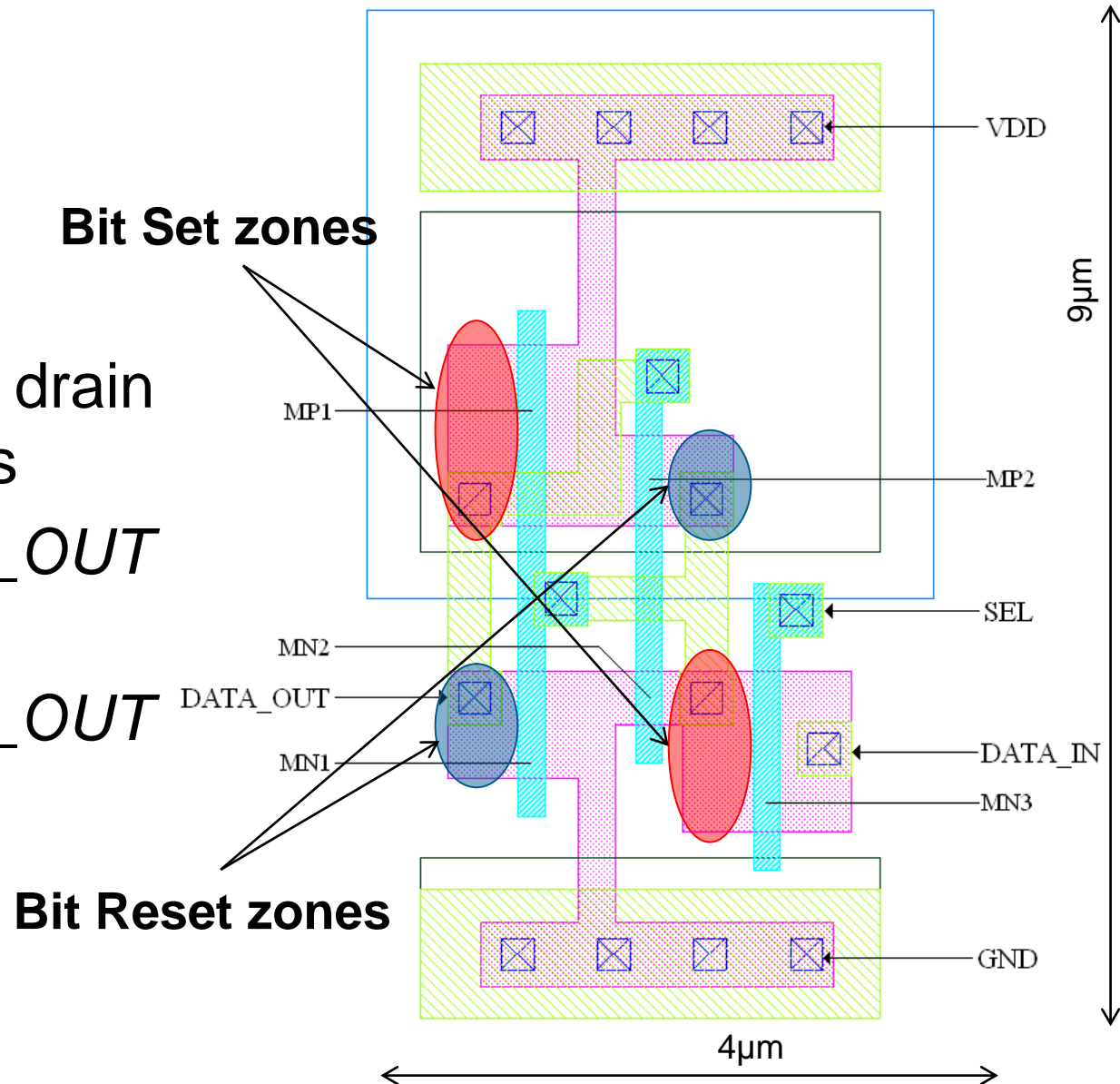
- Front side fault injection
- 1064nm wavelength
- Spot size: 1 μ m
- Pulse duration: 50 ns
- Energy from 1W to 1.6W
- SRAM grid pattern: 0.2 μ m





Sensitivity zones

- 4 theoretical zones
 - Corresponding to the drain of the OFF transistors
 - 2 zones when *DATA_OUT* is in high state ■
 - 2 zones when *DATA_OUT* is in low state ■

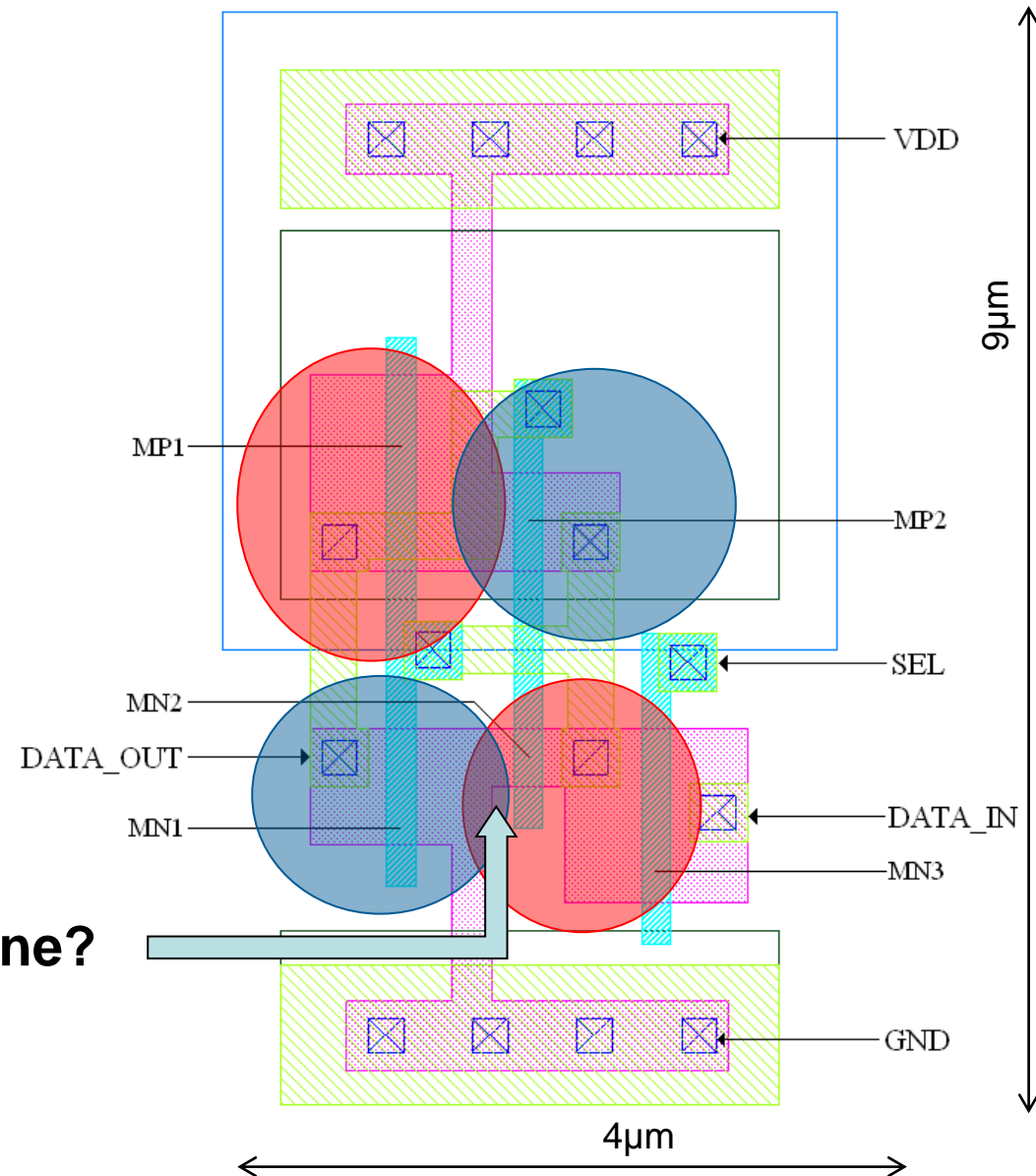




Sensitivity zones

- Laser spot size of $1\mu\text{m}$
 - Sensitivity zones extended
 - Bit set and reset zones overlap
 - For some positions: faults injected should be bit flip

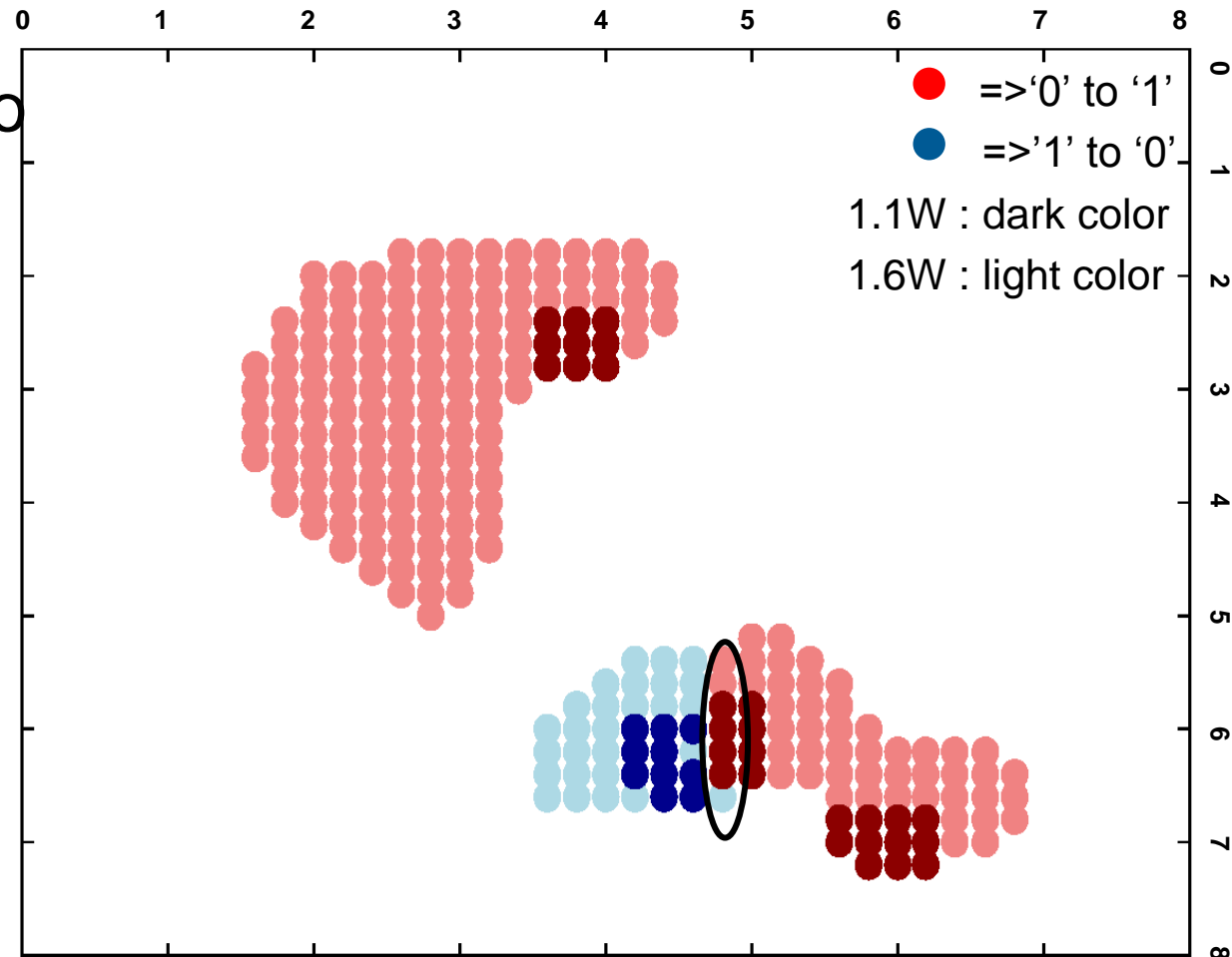
Bit flip zone?





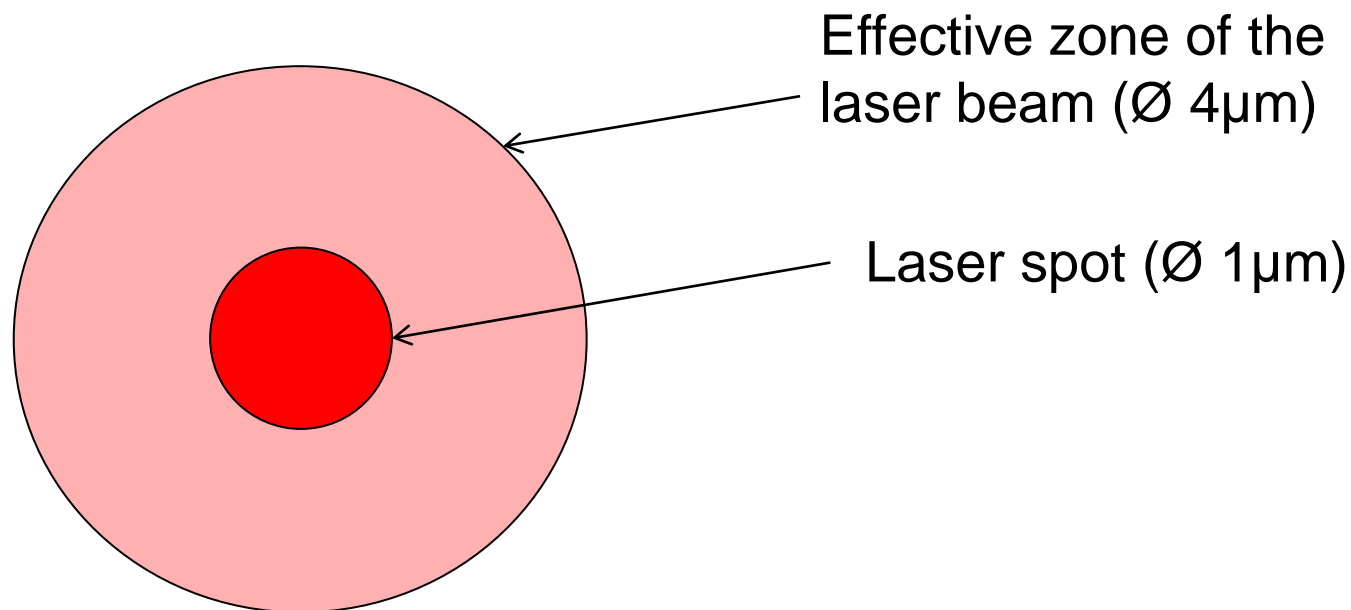
Sensitivity map of the memory cell

- Red zone and blue zone do not overlap.
- **No bit flip**
- Only 3 zones are really sensitive.
- **SPICE simulation on the edge zone**





- Based on the model of *Sarafianos et al.*[1]
 - Model developed with 90nm CMOS technology
 - Using Voltage controlled current source
 - Multiple current sources (several sensitive zones)

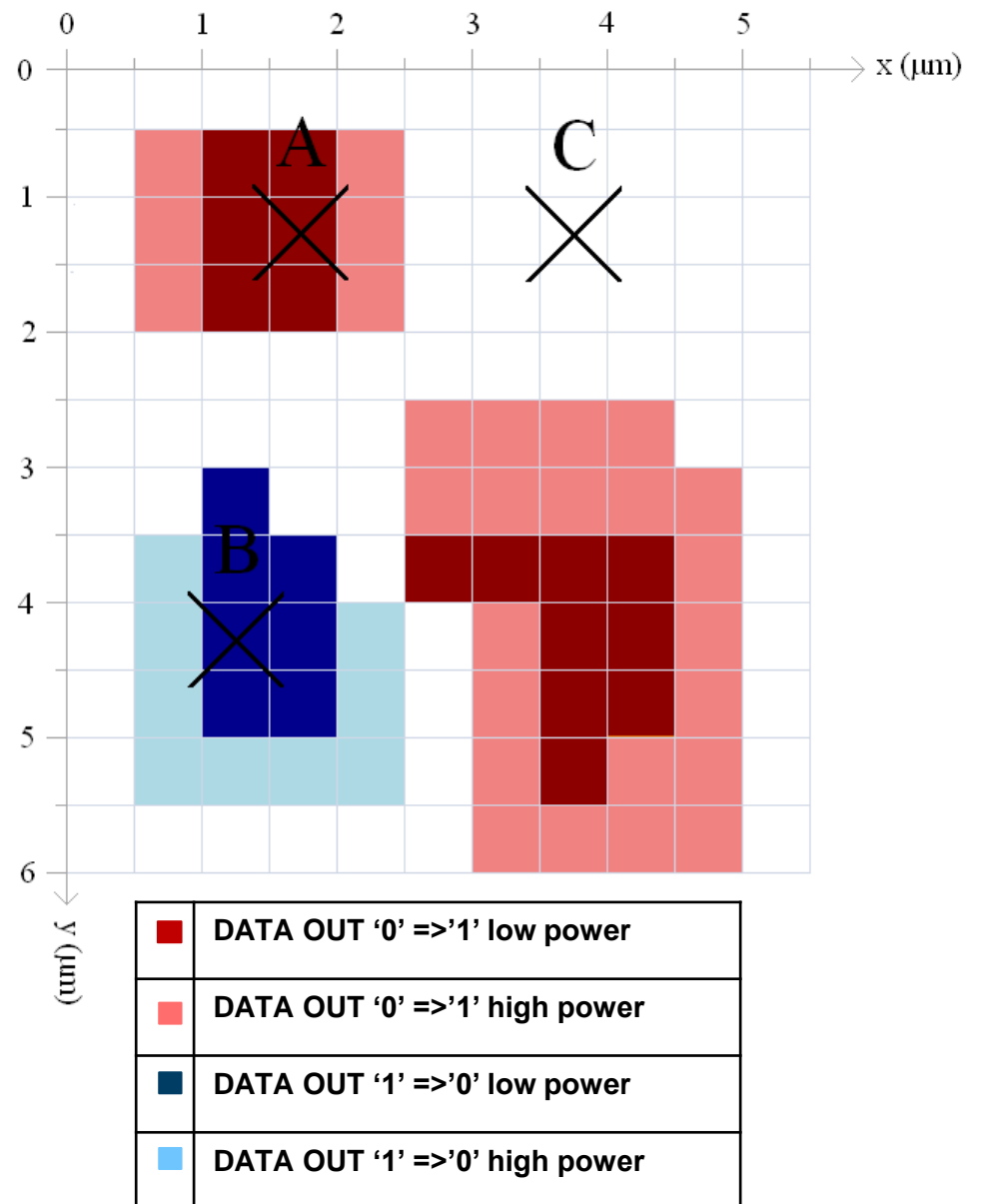


- The laser beam can reach several sensitivity zones of the cell



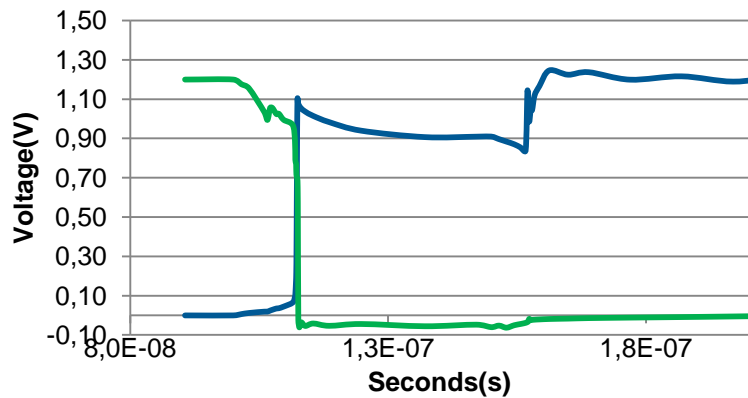
First simulation

- Similar to the experiments
- Same hidden zone
- No bit flip

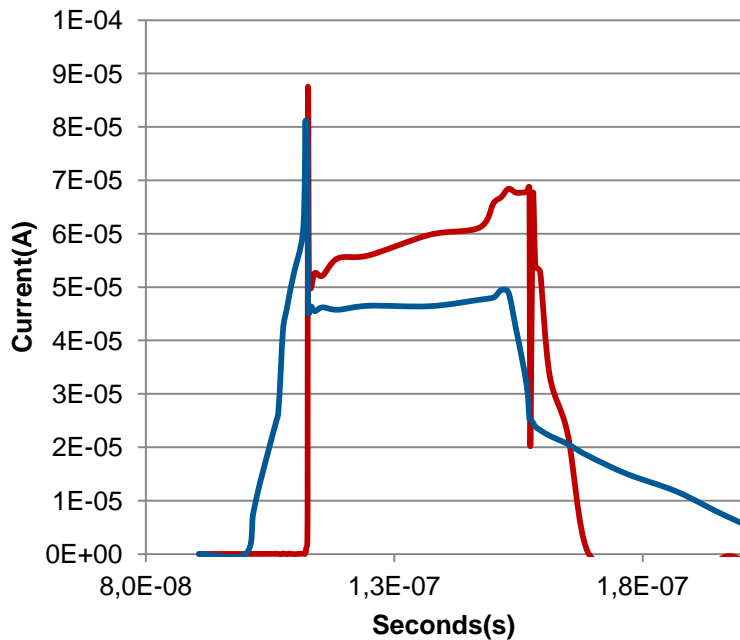




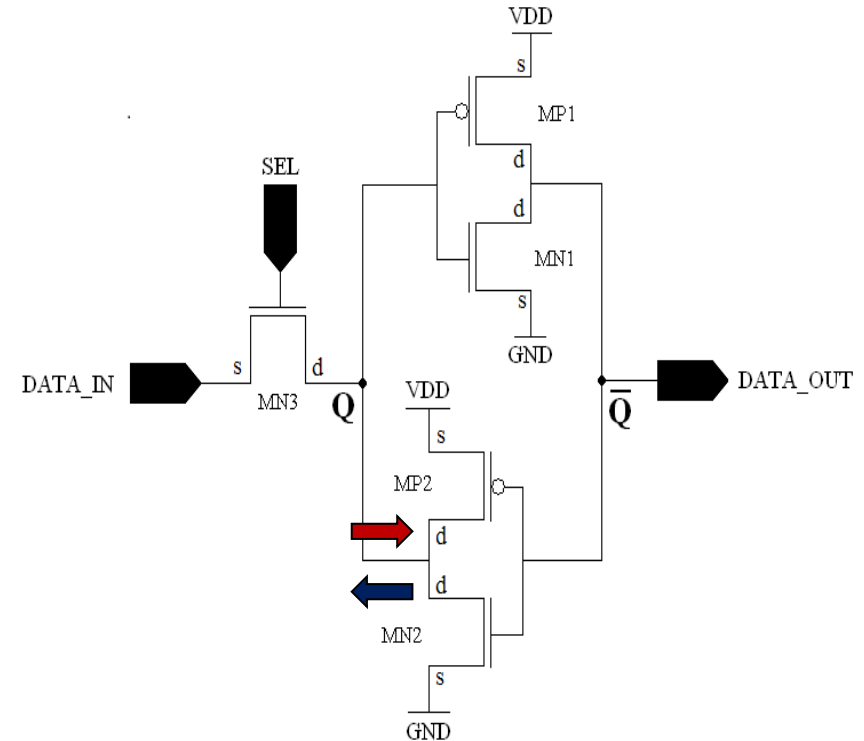
Simulation of the edge zone



— DATA_OUT
— Q



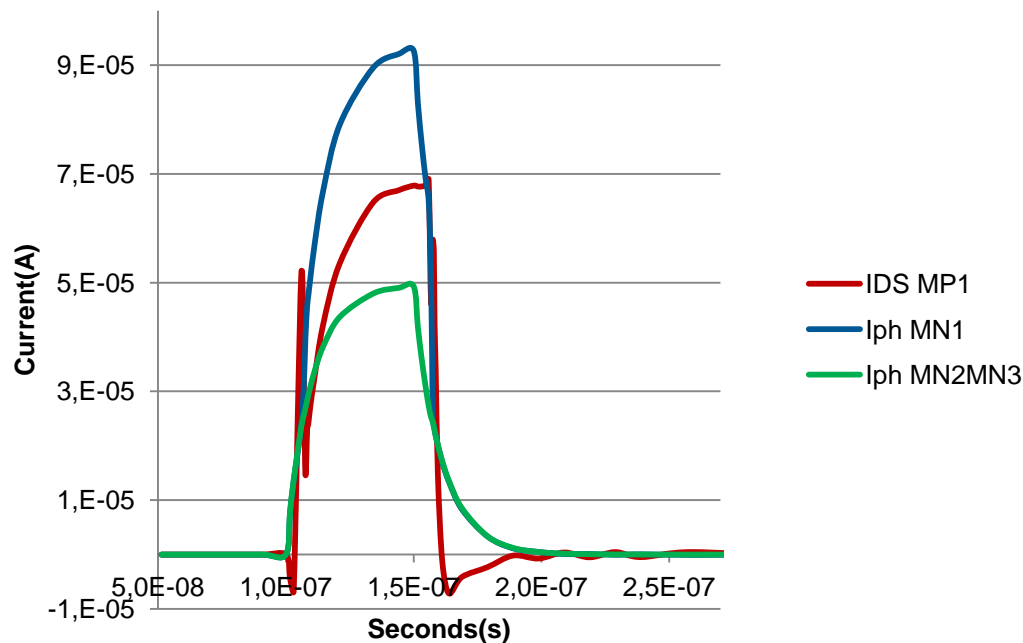
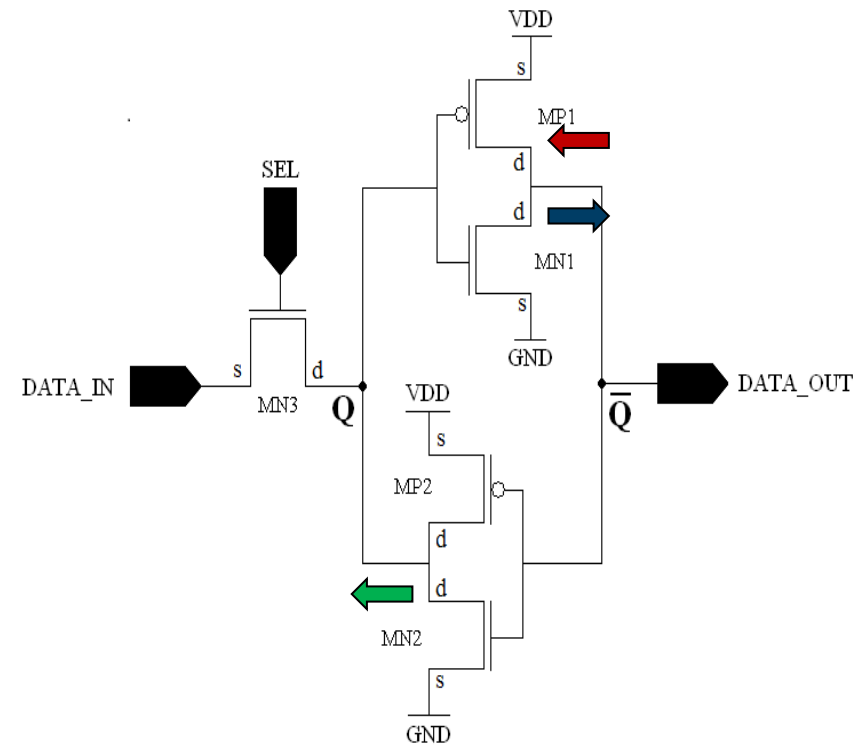
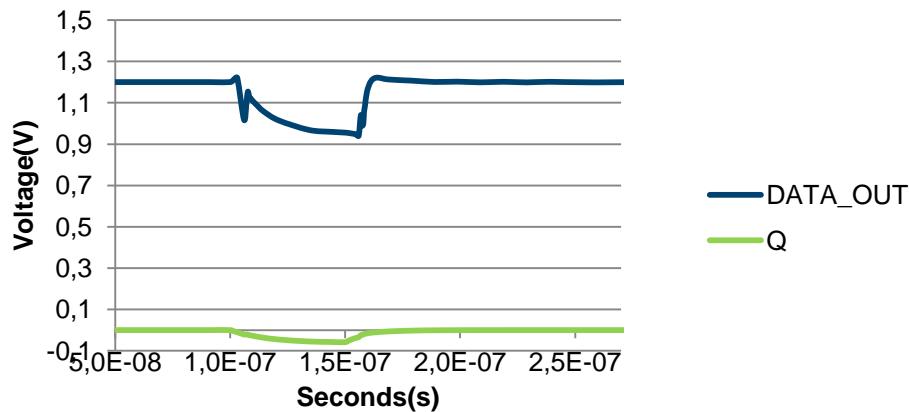
— IDS MP2
— iph MN2MN3



- Current injected on the drain of MN2
- Current of MP2 in opposition
- State has already changed
- **Fault is injected (bit set)**



Simulation of the edge zone



- Current injected in drain of MN1
- Two other current are in opposition
- **No fault injected**



- **No bit flip**
 - Despite the laser beam effect zone (\emptyset 1 μ m & 5 μ m)
 - Energy between 1W and 1.6W
 - Balanced current that avoid fault
- **Good correlation between simulation and experimentation**
 - Same edge zone
 - Analyze the hidden zone
 - Countermeasures will be investigated in future works



Thank you for your attention.

Questions?

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