DE LA RECHERCHE À L'INDUSTRIE

cea

INSPIRING INNOVATION | INNOVANTE PAR TRADITION

Ecole Nationale Supérieure des Mines SAINT-ETIENNE

Cosade 2013

From physical stresses to timing constraints violation

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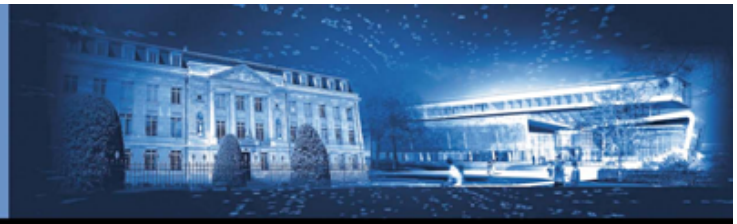
Introduction

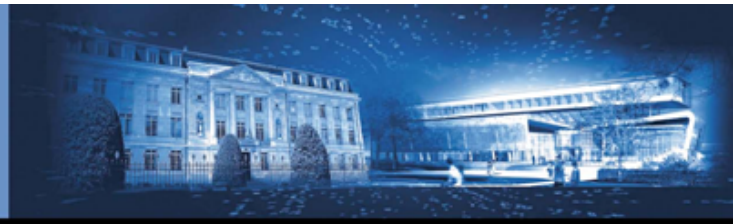


Research subject

- **Caracterization and analysis of common fault injection mechanism**

Today's subject

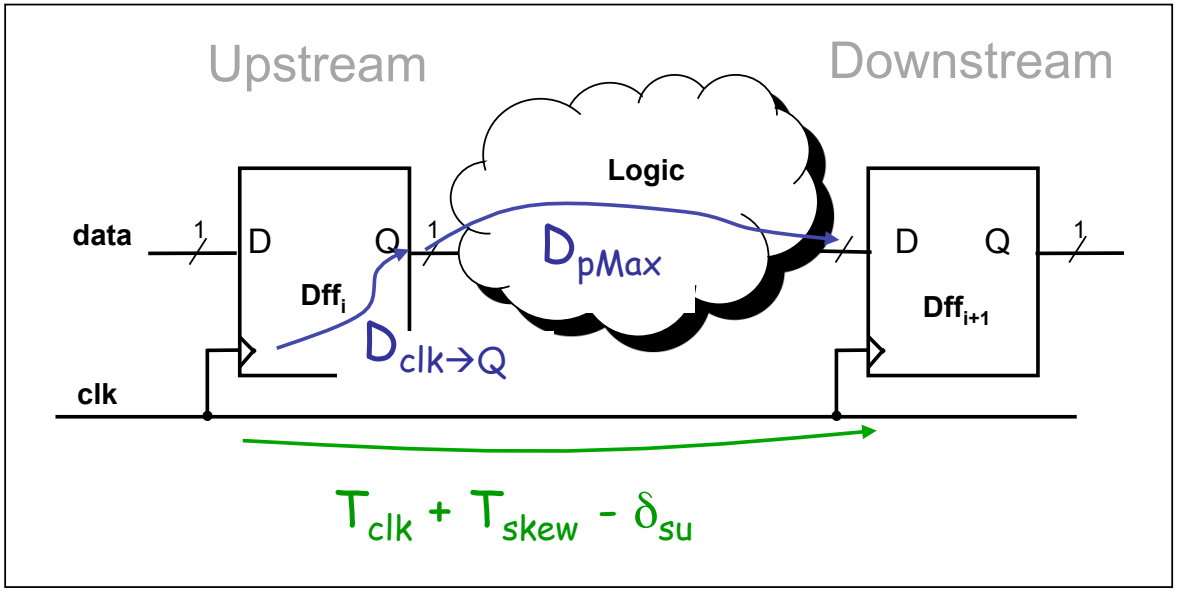
- **Power glitches fault injection mechanism**
  - **Analysis and practice**



Agenda

- **Timing constraints of synchronous digital IC**
- **Static stresses (global effect)**
- **Transient stresses**
- **Conclusion**

Timing constraints

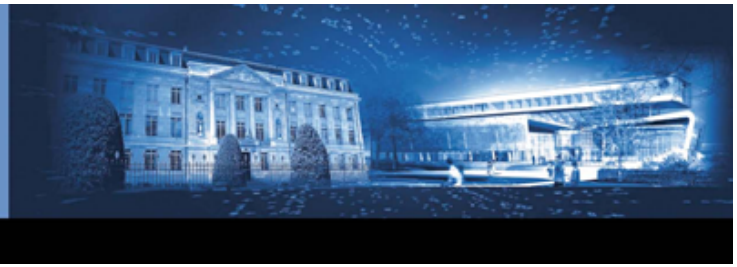


data arrival time = $D_{clk \rightarrow Q} + D_{pMax}$

data required time = $T_{clk} + T_{skew} - \delta_{su}$

$\Rightarrow$ $T_{clk} > D_{clk \rightarrow Q} + D_{pMax} - T_{skew} + \delta_{su}$

Timing constraints violation



How to inject faults through timing constraints violation?

- Overclocking: (Frequency increase, i.e. period decrease)

$$T_{clk} < D_{clk \rightarrow Q} + D_{pMax} - T_{skew} + \delta_{su}$$

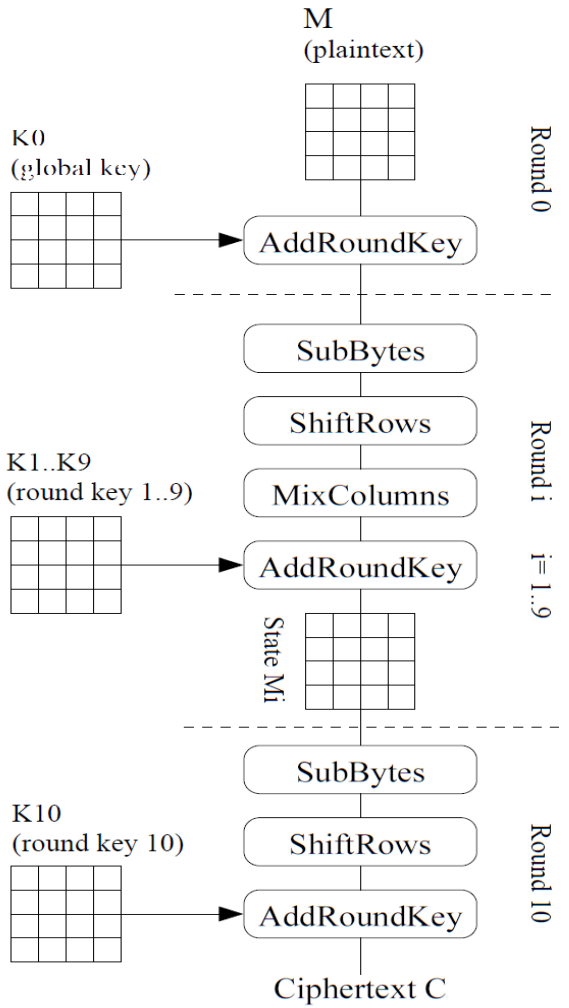
- Underpowering or overheating: (Propagation time increase)

$$T_{clk} < D_{clk \rightarrow Q} + D_{pMax} - T_{skew} + \delta_{su}$$

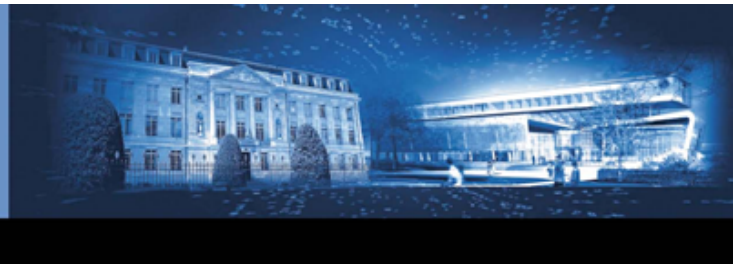
Experimental setup

Target

- Platform: FPGA Spartan 3A
- Algorithm: AES 128 bit
  none-secure implementation
- Frequency: 100 MHz
- Power supply: 1.2V



Previous research work



Common fault injection means

- Clock stress (overclocking)
- Power stress (underpowering)
- Overheating

A **common mechanism** !

⇒ Timing constraints violations.

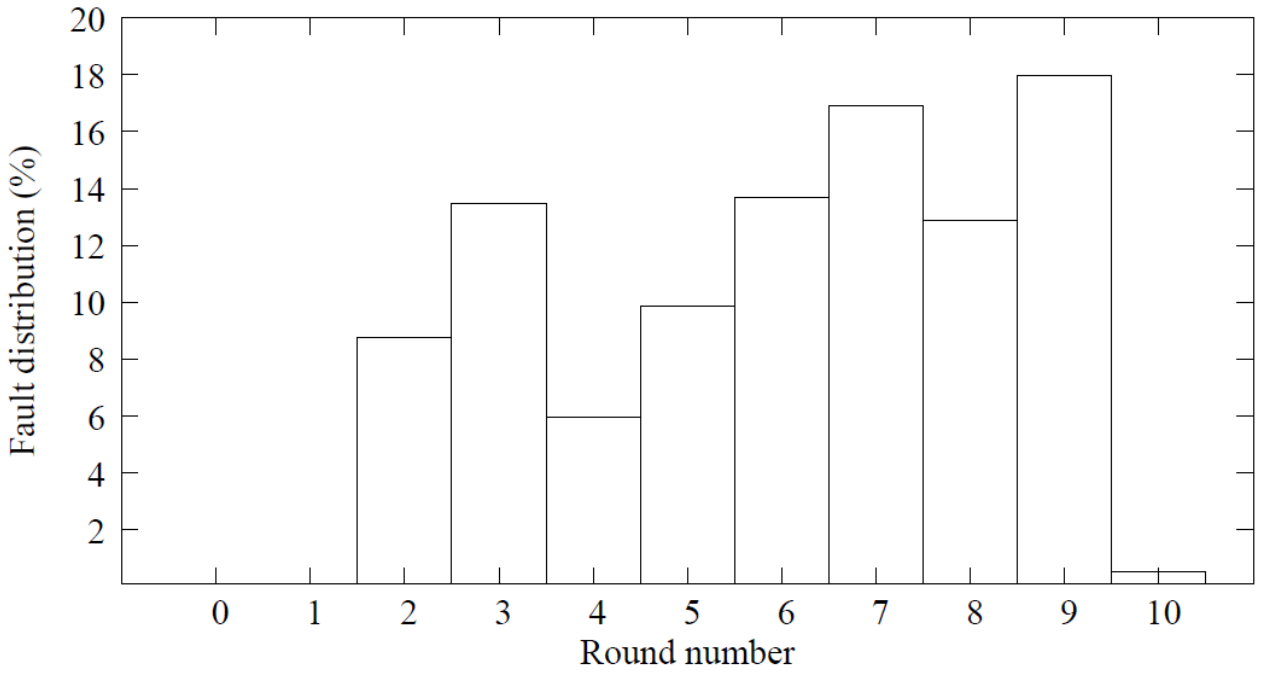
Experimental proof

- 10,000 input dataset
- Critical path faulted

Static perturbations

Issues

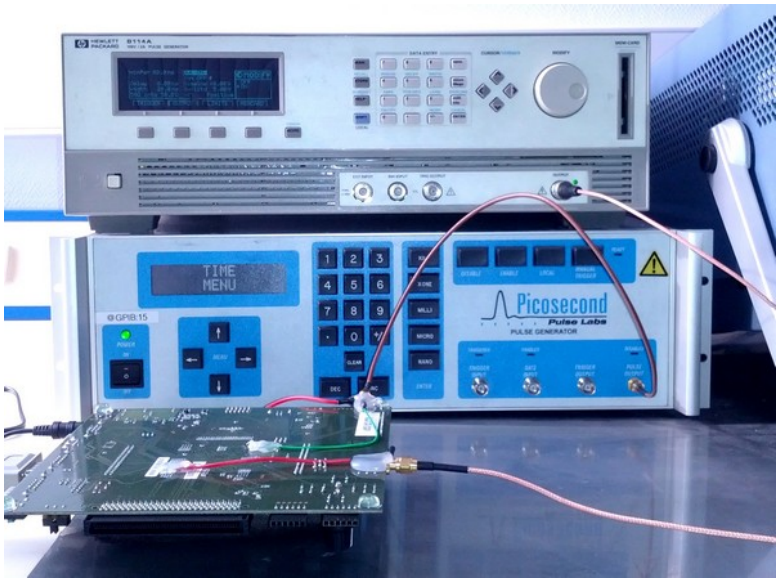
- Low timing resolution



Transient perturbations

Transient perturbations

- Clock glitch
- Power supply glitch

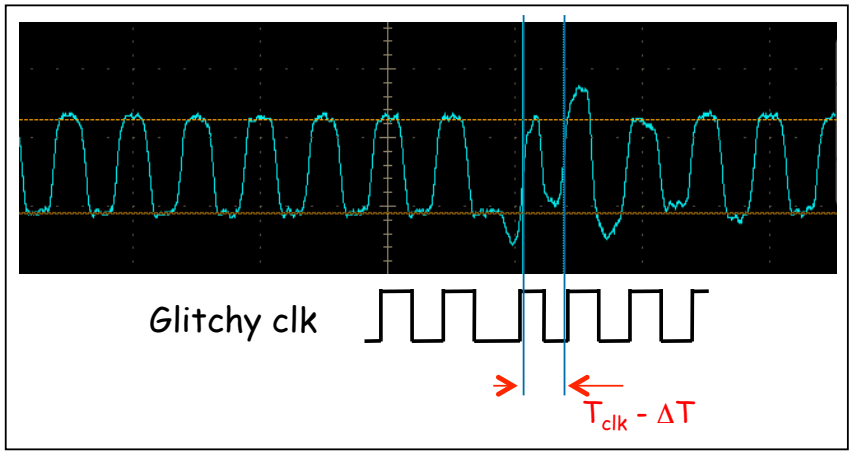


Questions

- Injection mechanism? Timing violation?
- Achievable resolution?

Transient perturbations

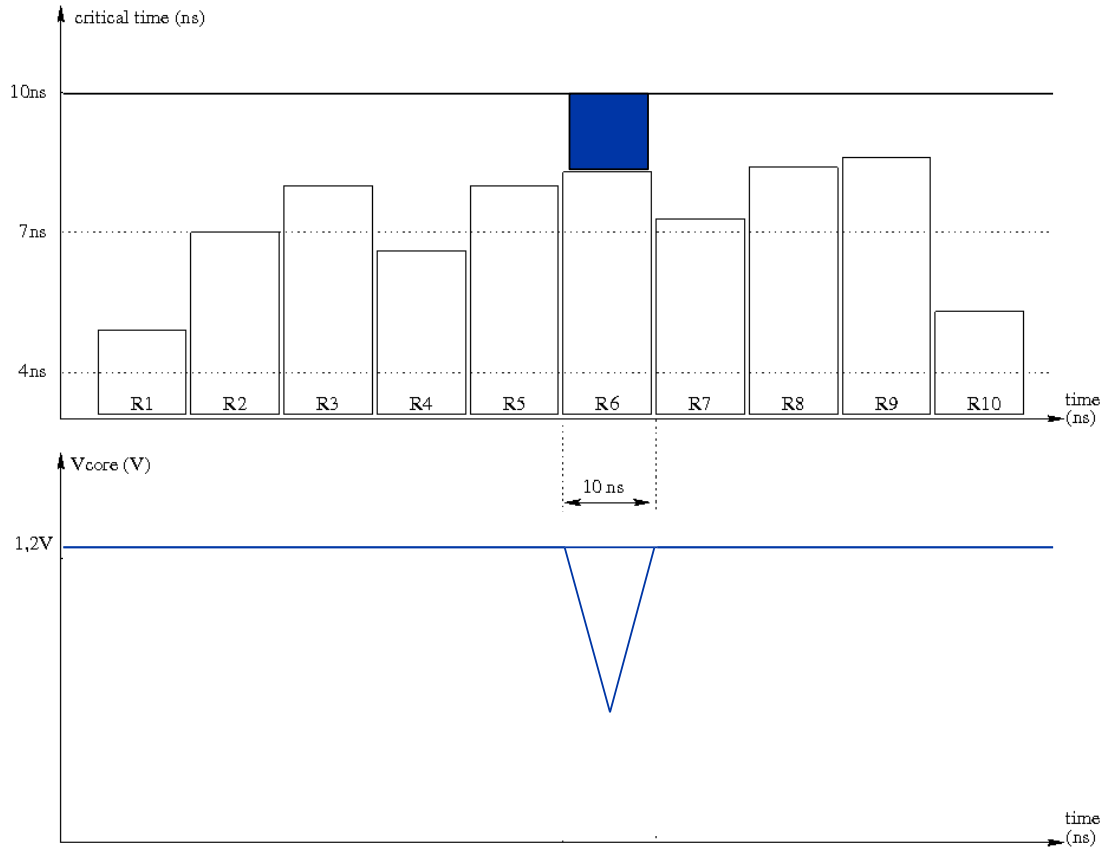
Clock glitch



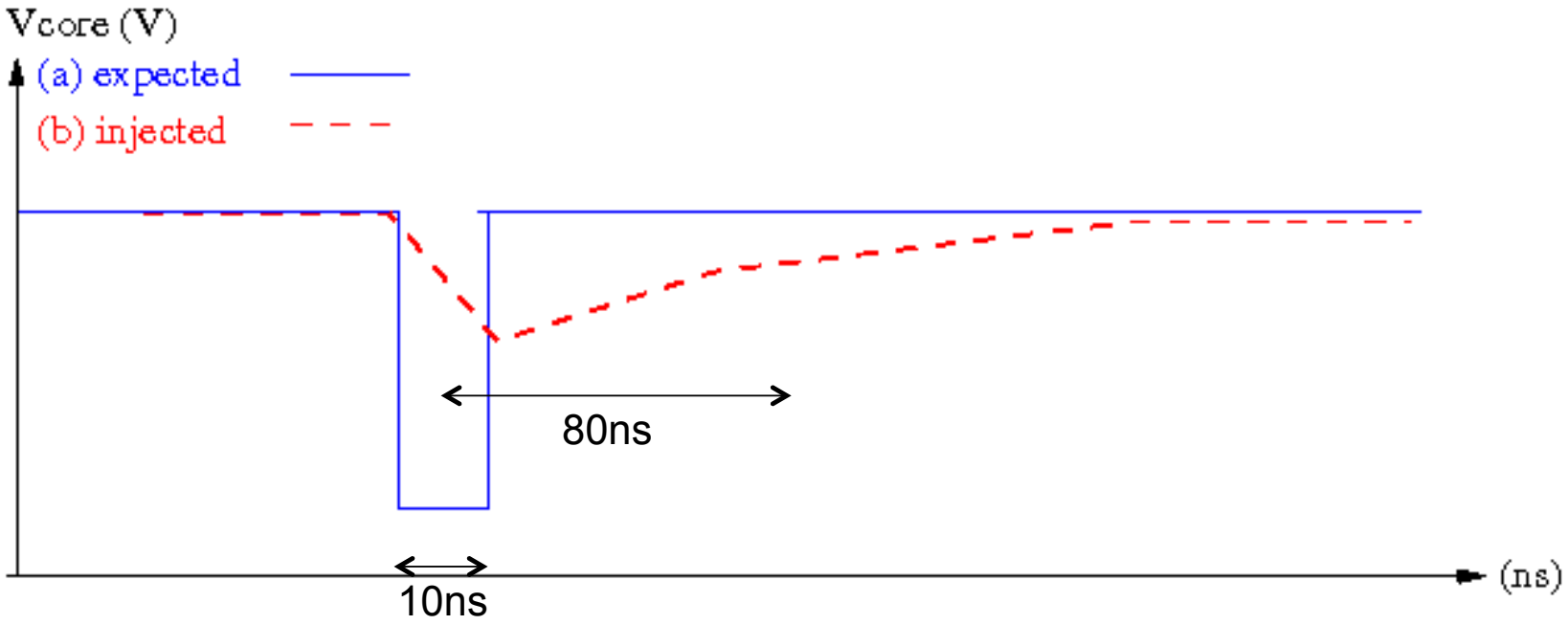
- 35ps resolution
- Global effect
- Timing constraints violation (obvious)
- A tool for critical time measurement
- Used to build a template/**reference library**

To be compared,

Power glitch: Ideal

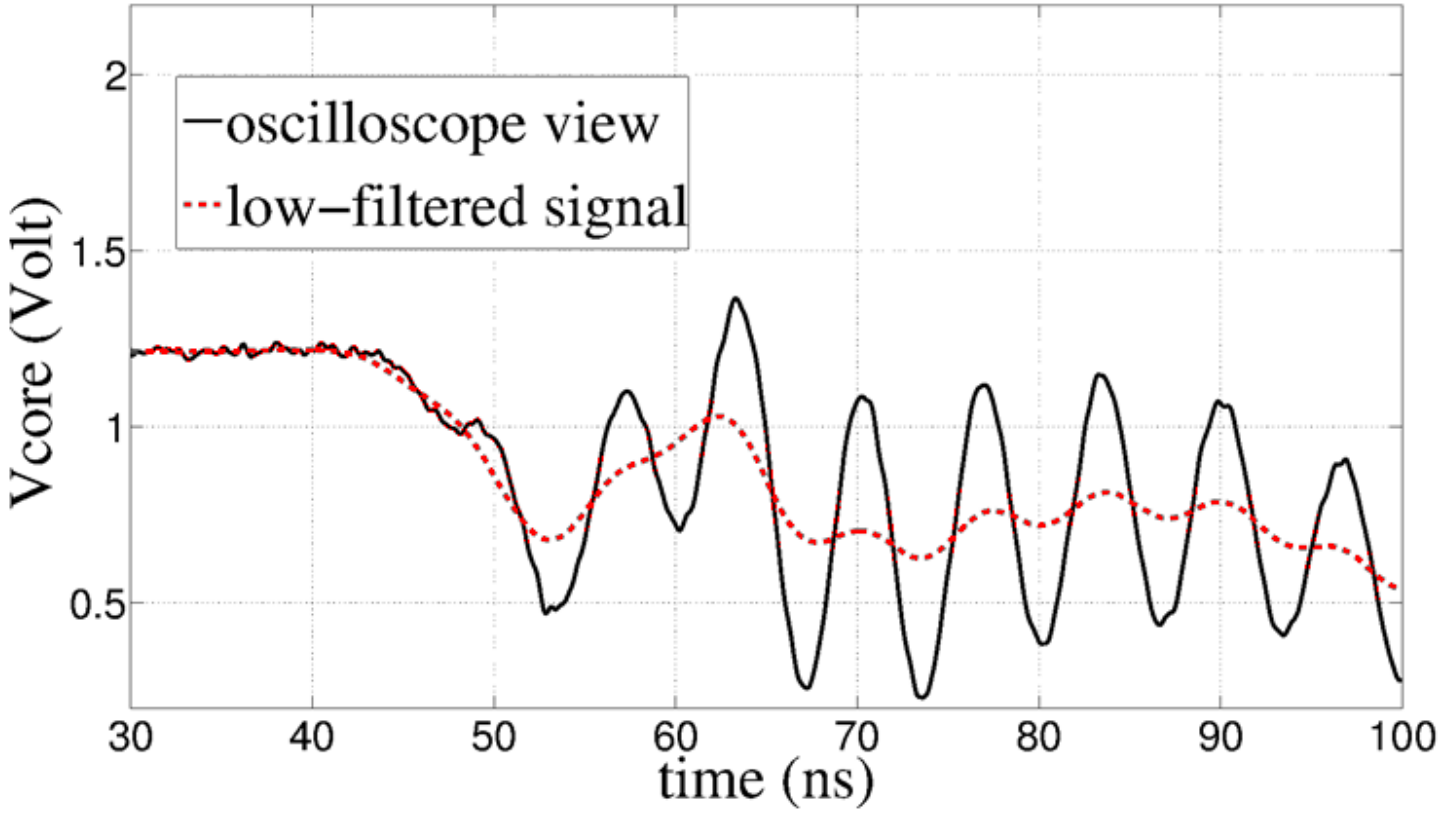


Power glitch: Input capacitance

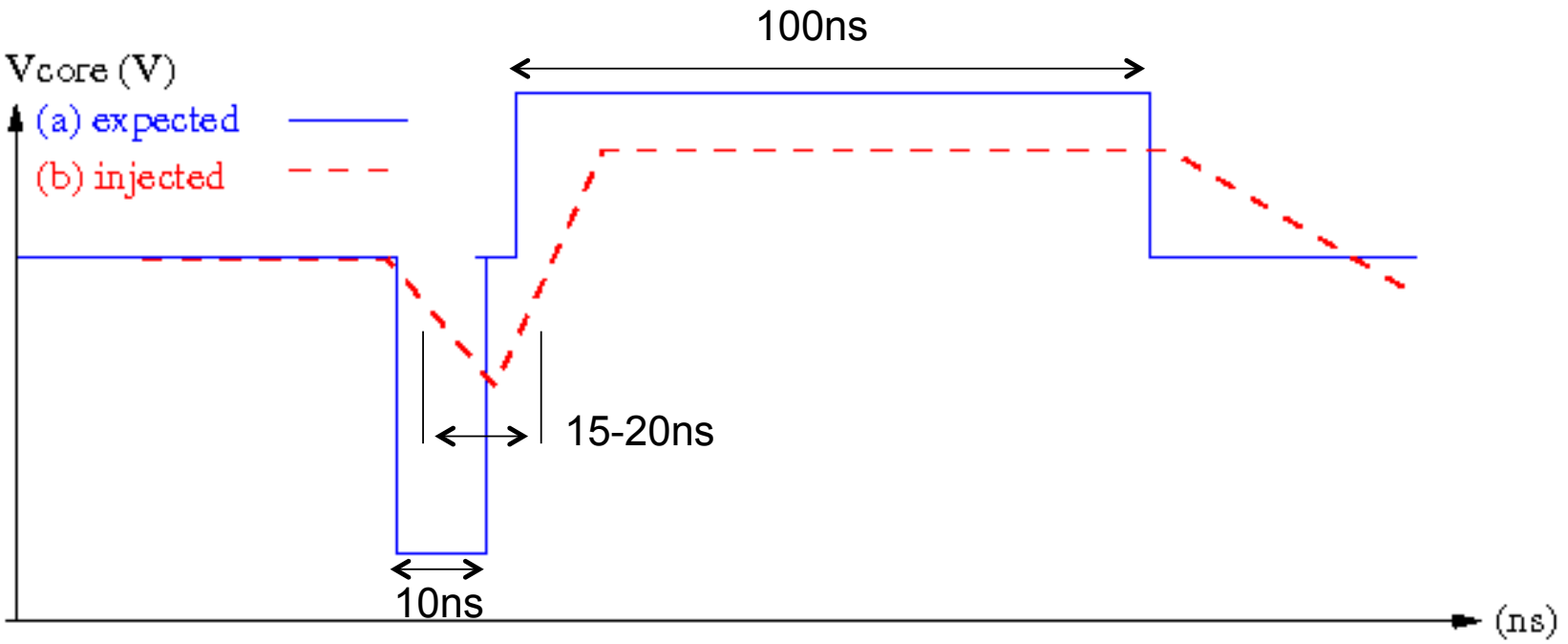


Transient perturbations

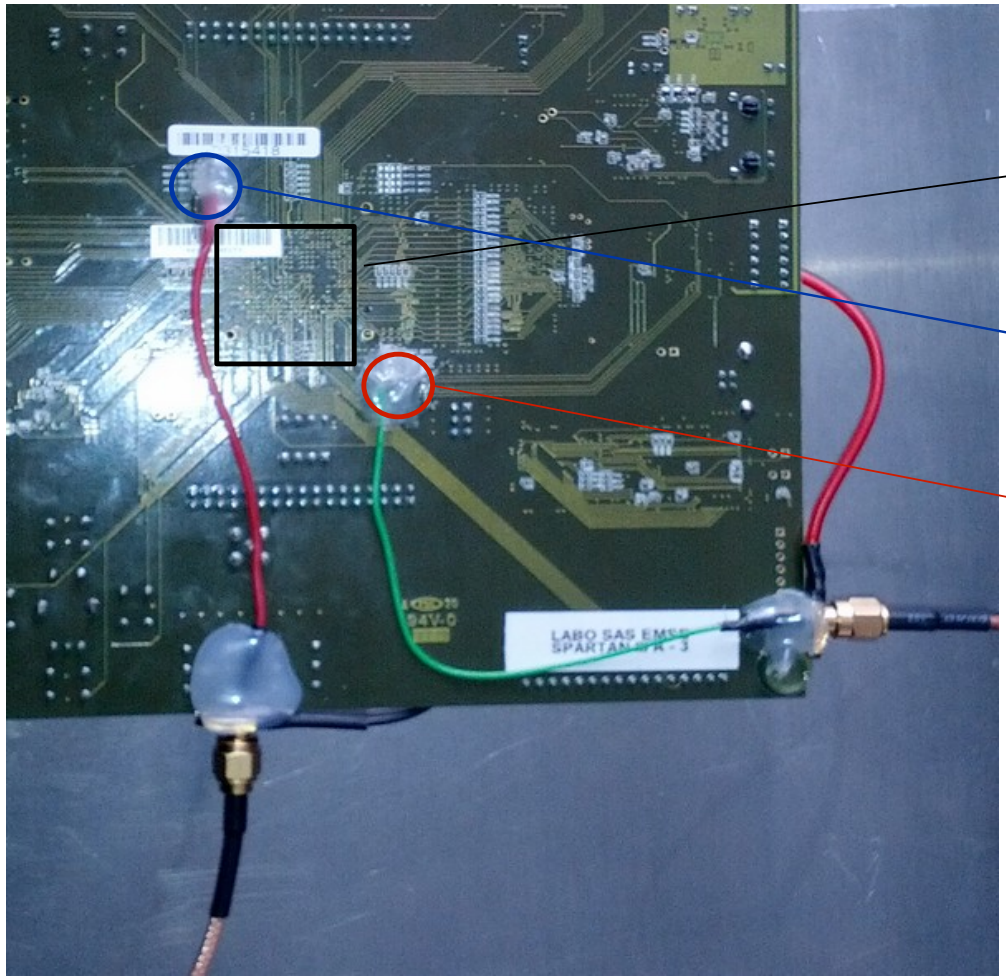
Power glitch: impedance adaptation



Power glitch: Input capacitance

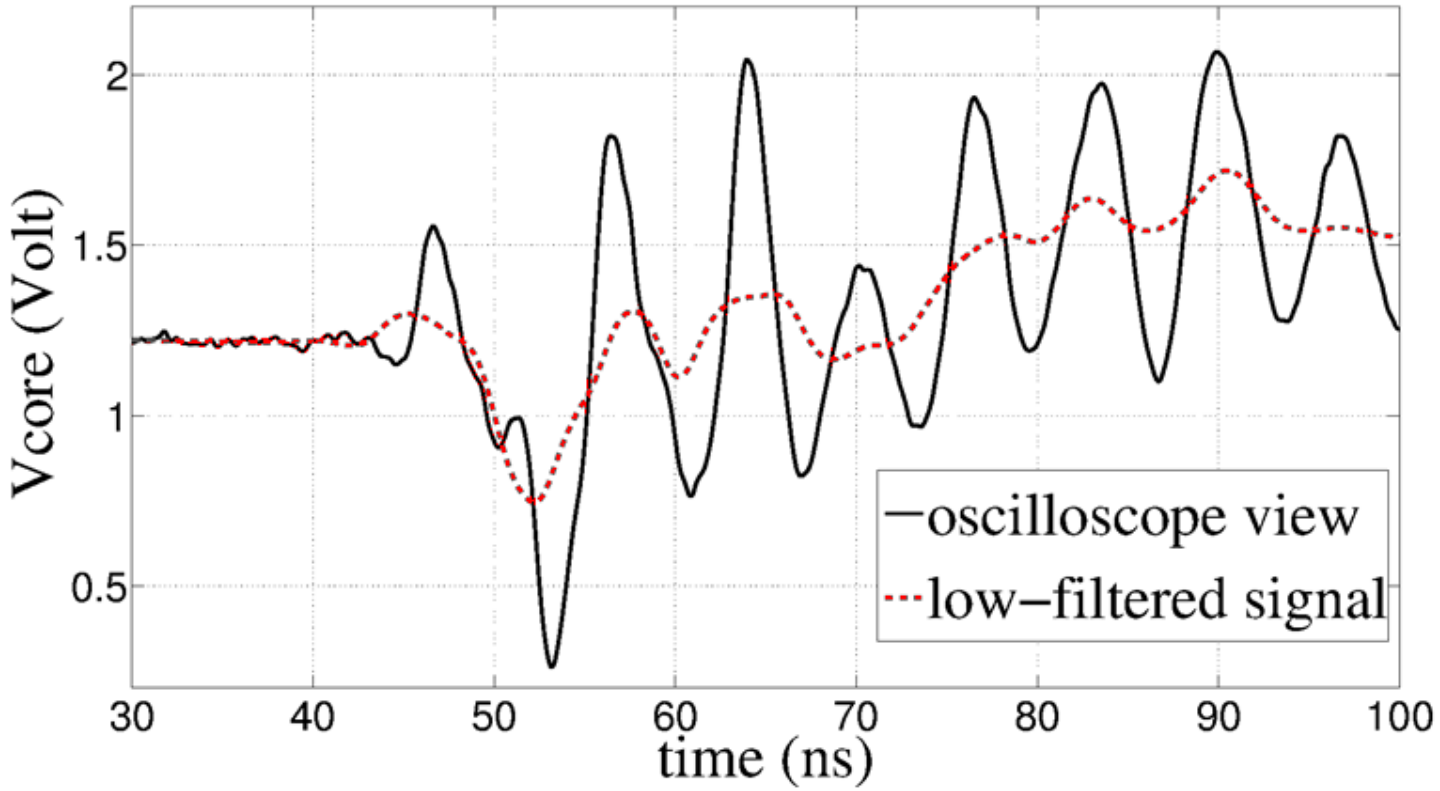


Transient perturbations



Transient perturbations

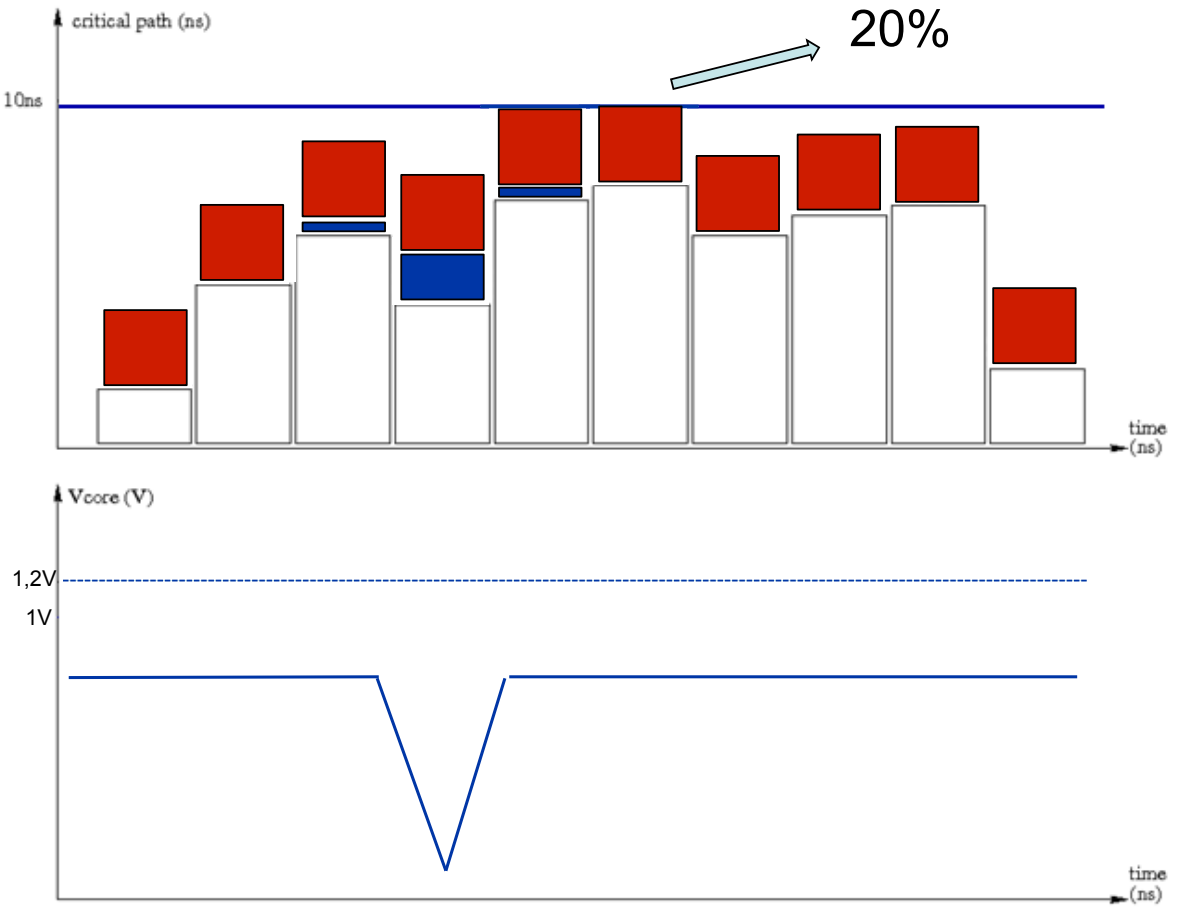
Power glitch: impedance adaptation



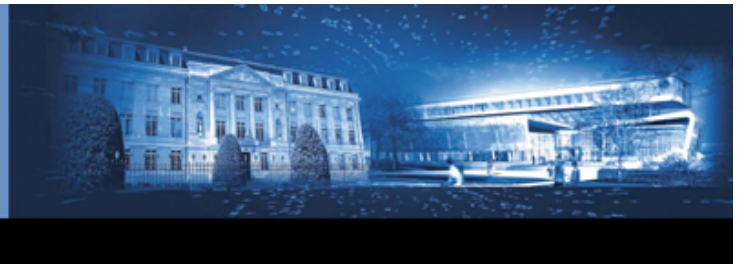
Transient perturbations

Power glitch

- Target a specific round but **also affect the neighboring rounds,**
- Global offset must be added.



Conclusion



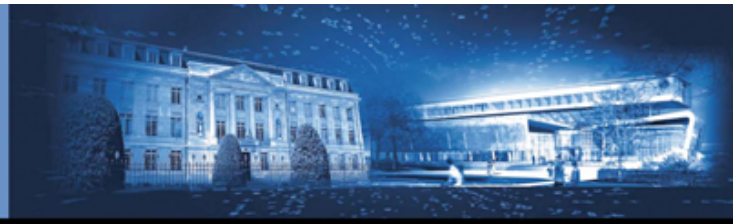
Power glitch

- Analysis of injected faults:
  - 70% identical to clock glitch injection
  - 20% neighboring rounds
  - 10% the second most critical path of the round
- Conclusion: Clock and power glitch induced faults are due to timing constraints violation
- >90% single-bit fault

A spatial effect component?

Linked to voltage transient propagation through the power supply grid

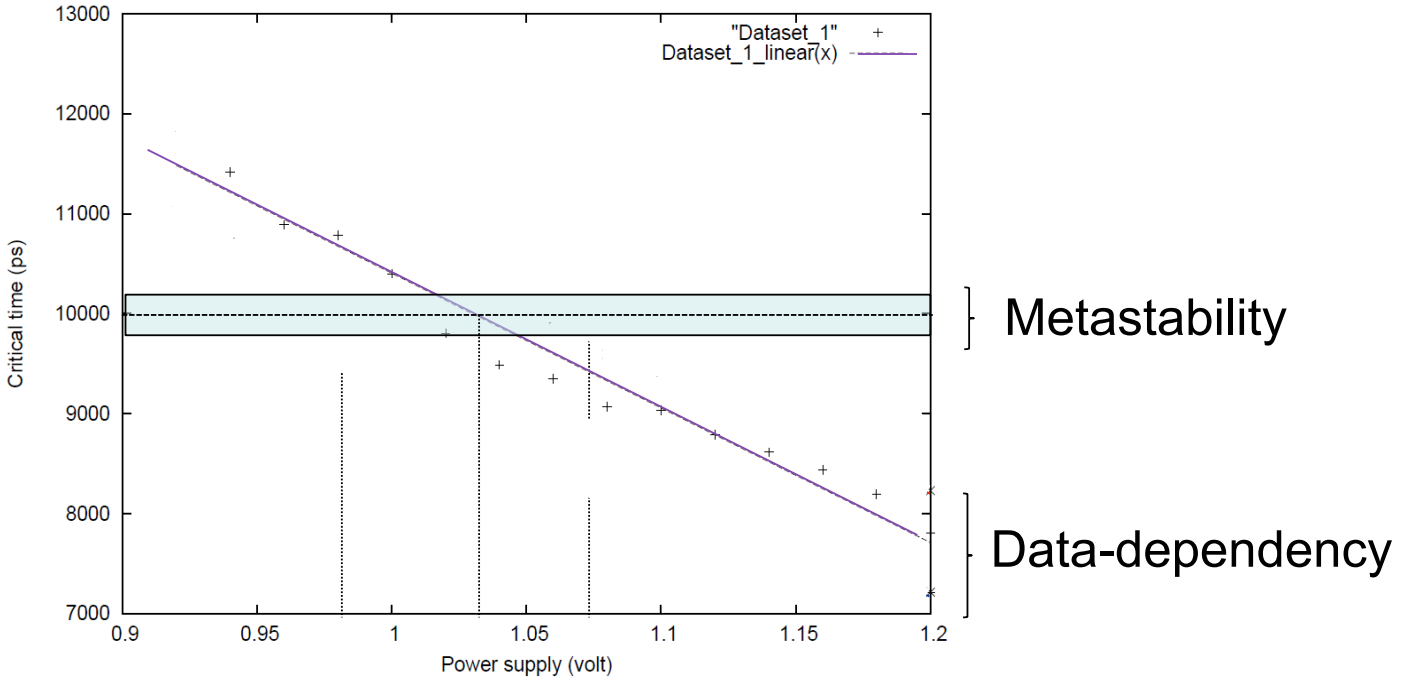
Questions



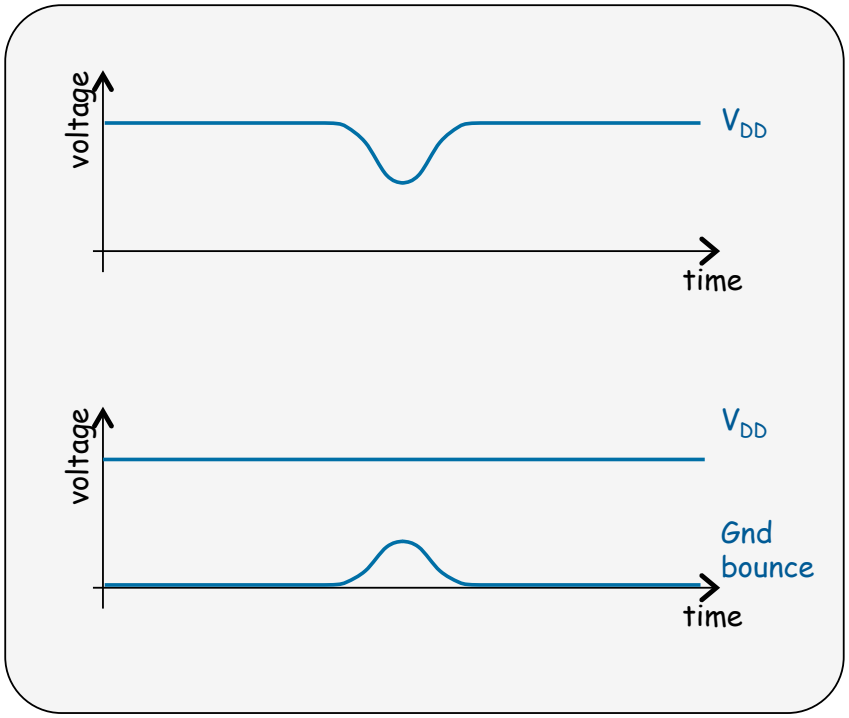
Static perturbations

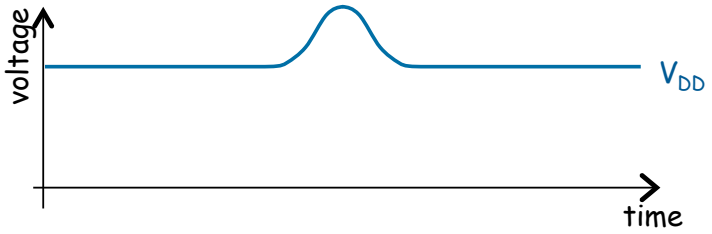
Underpowering

- Voltage decrement => critical path increase



Power glitch

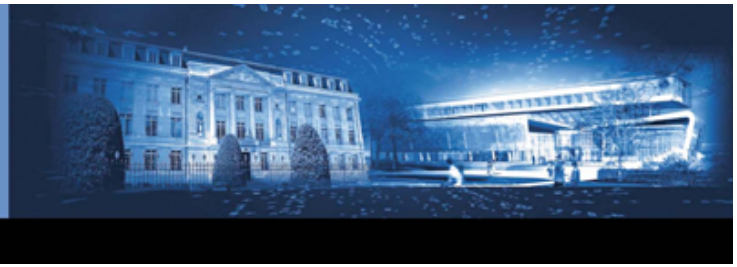




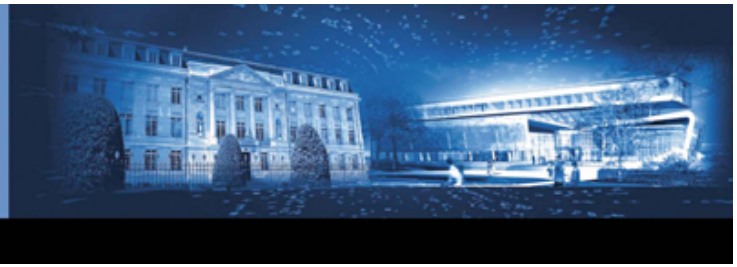
- Injection mechanism?

=> Timing violation

Conclusion

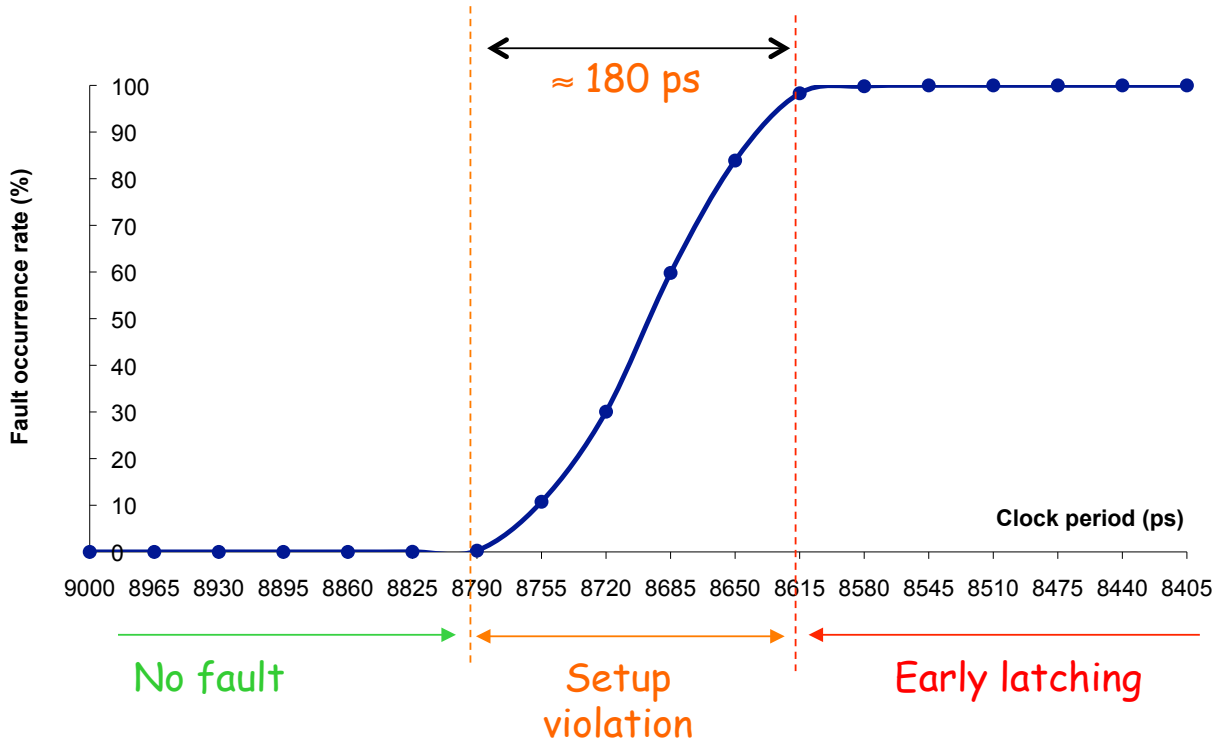


- **Overclocking, underpowering, overheating** generate exactly the sames faults => **same mechanism**,
- **Static stresses** give **accurate results** BUT **random temporal localization**,
- **Transient stresses** give a **better temporal localization** BUT inducing **spactial effect**,
- Indepth investigation are going to explain these spatial effects.



Overclocking

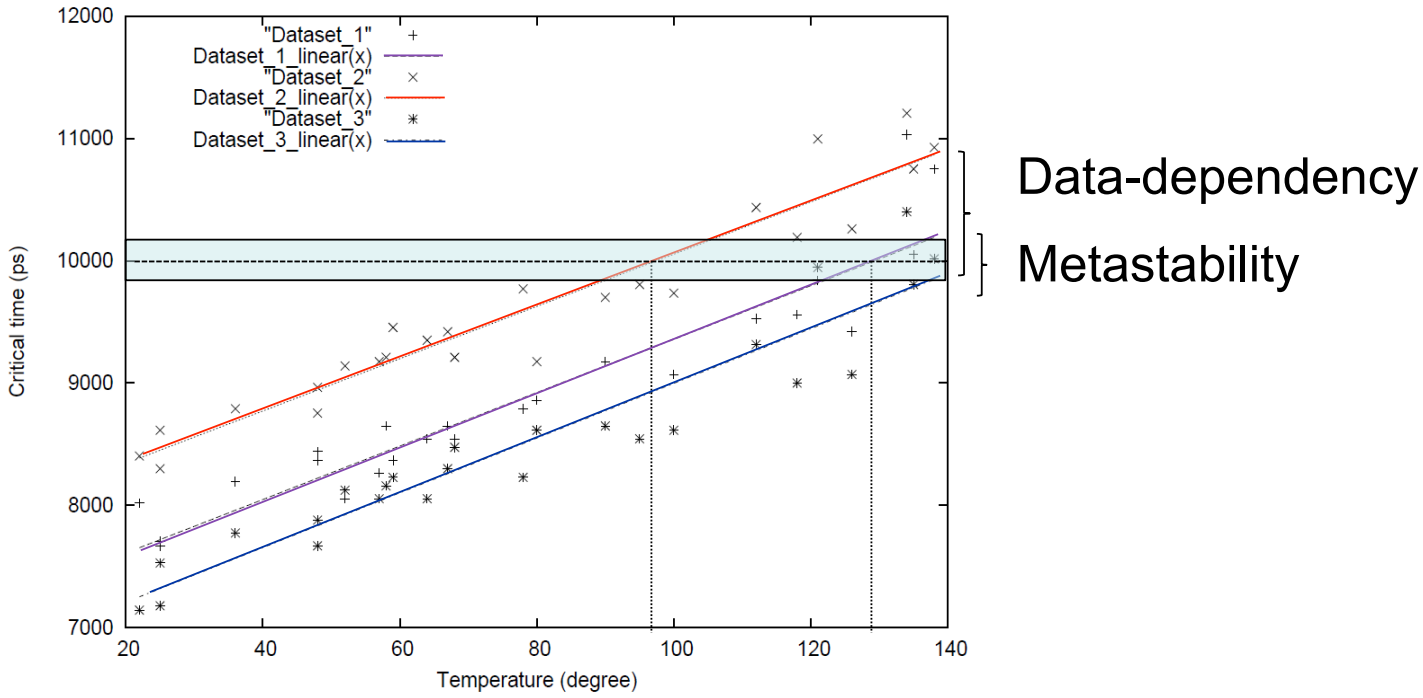
- Fault occurrence rate vs applied stress



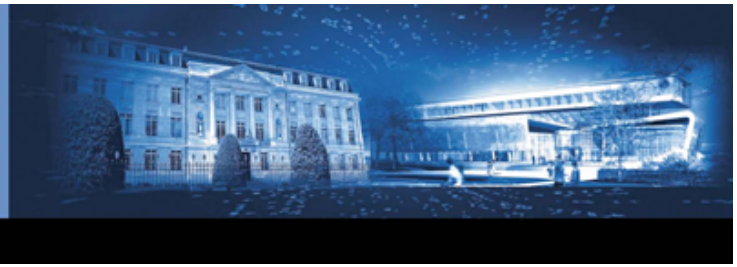
Static perturbations

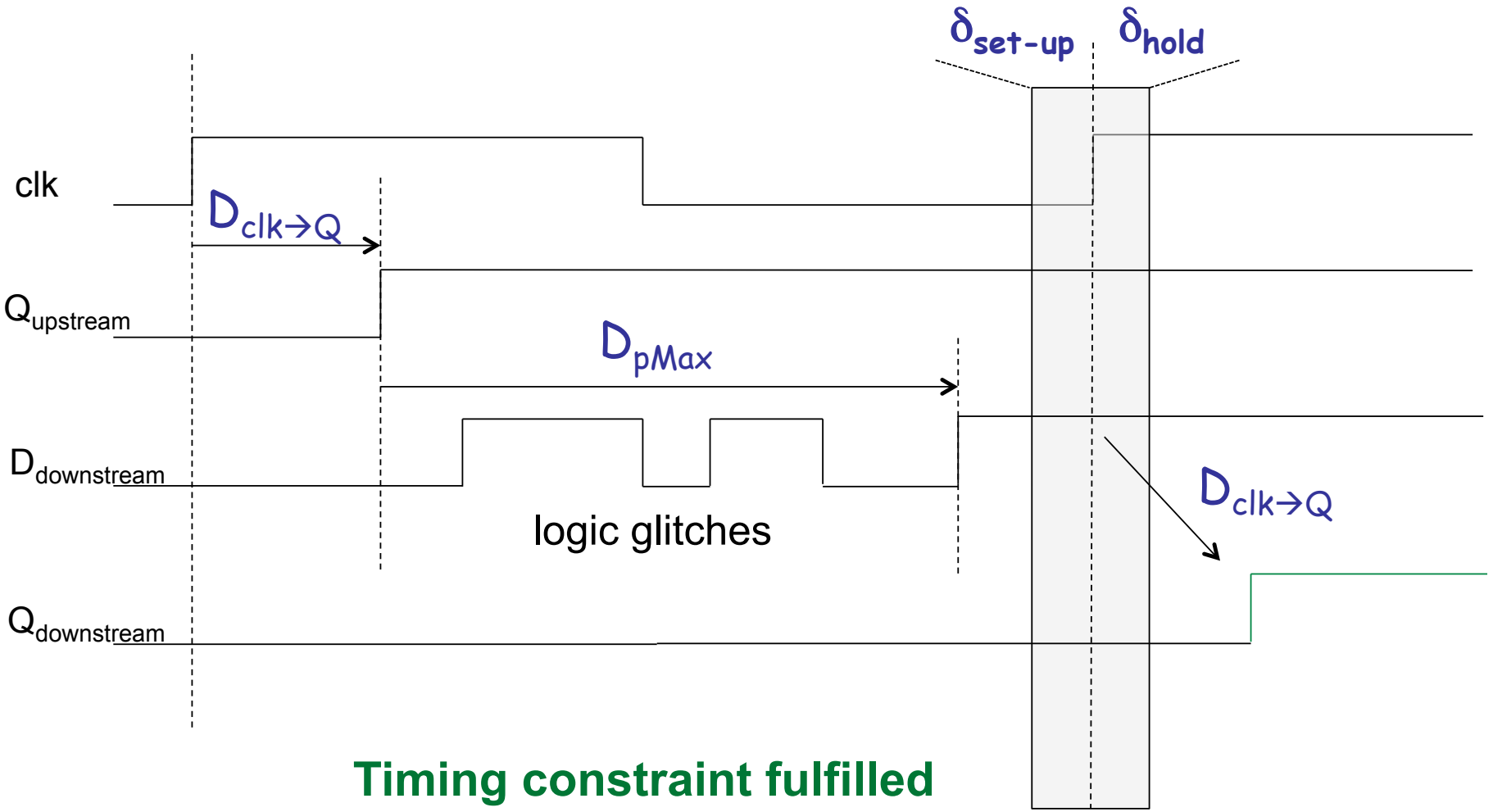
Overheating

- Temperature increase => critical path increase



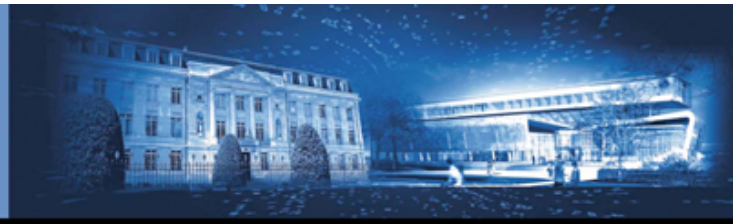
Overclocking

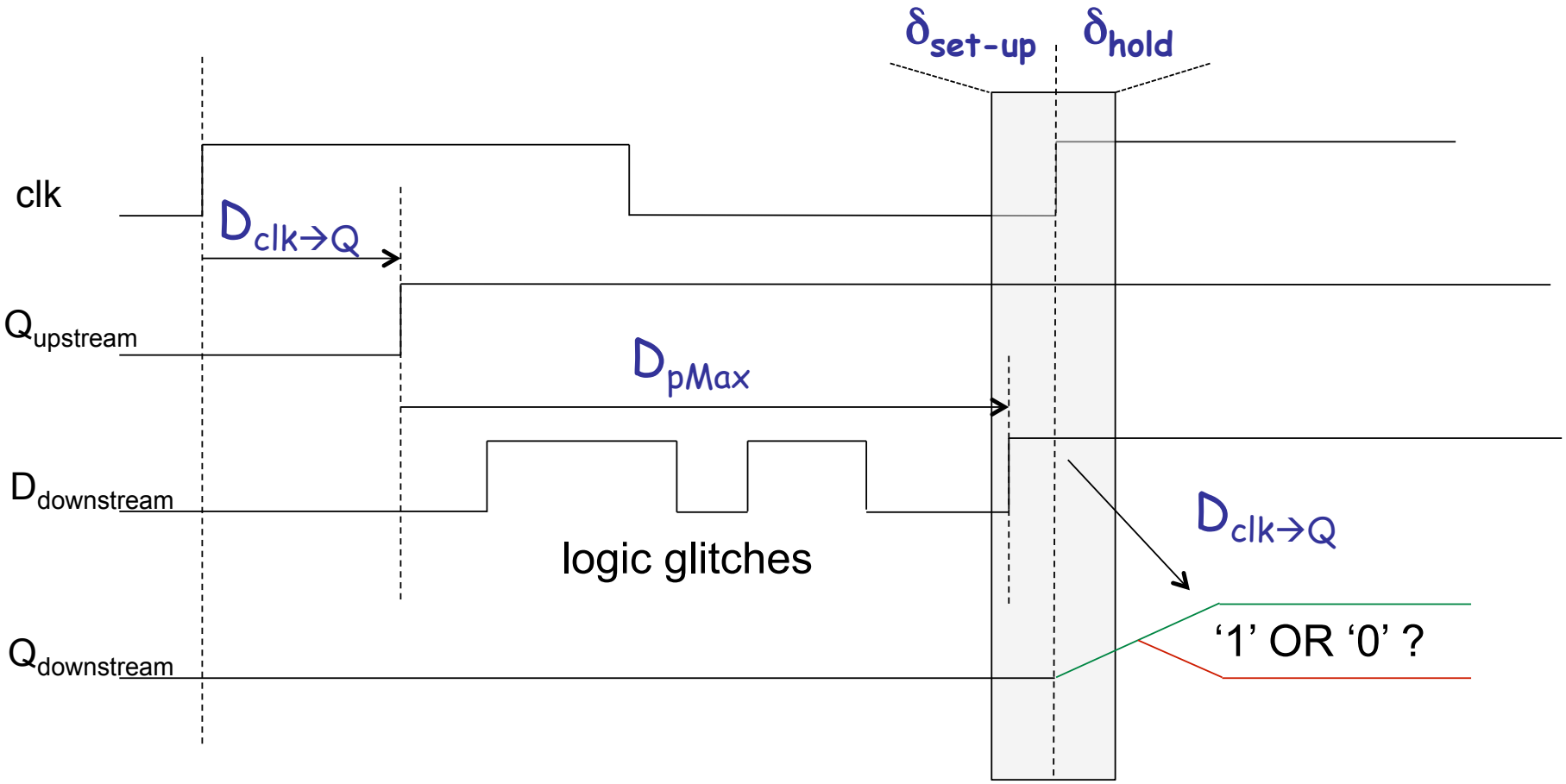




Timing constraint fulfilled

Overclocking

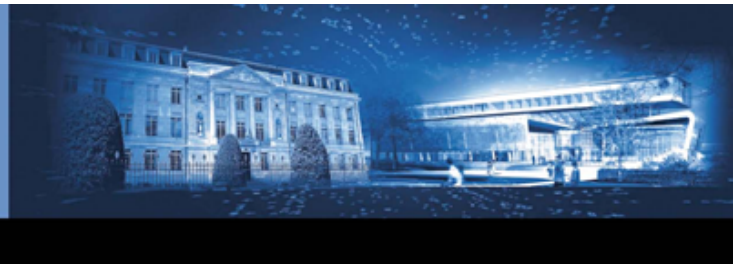


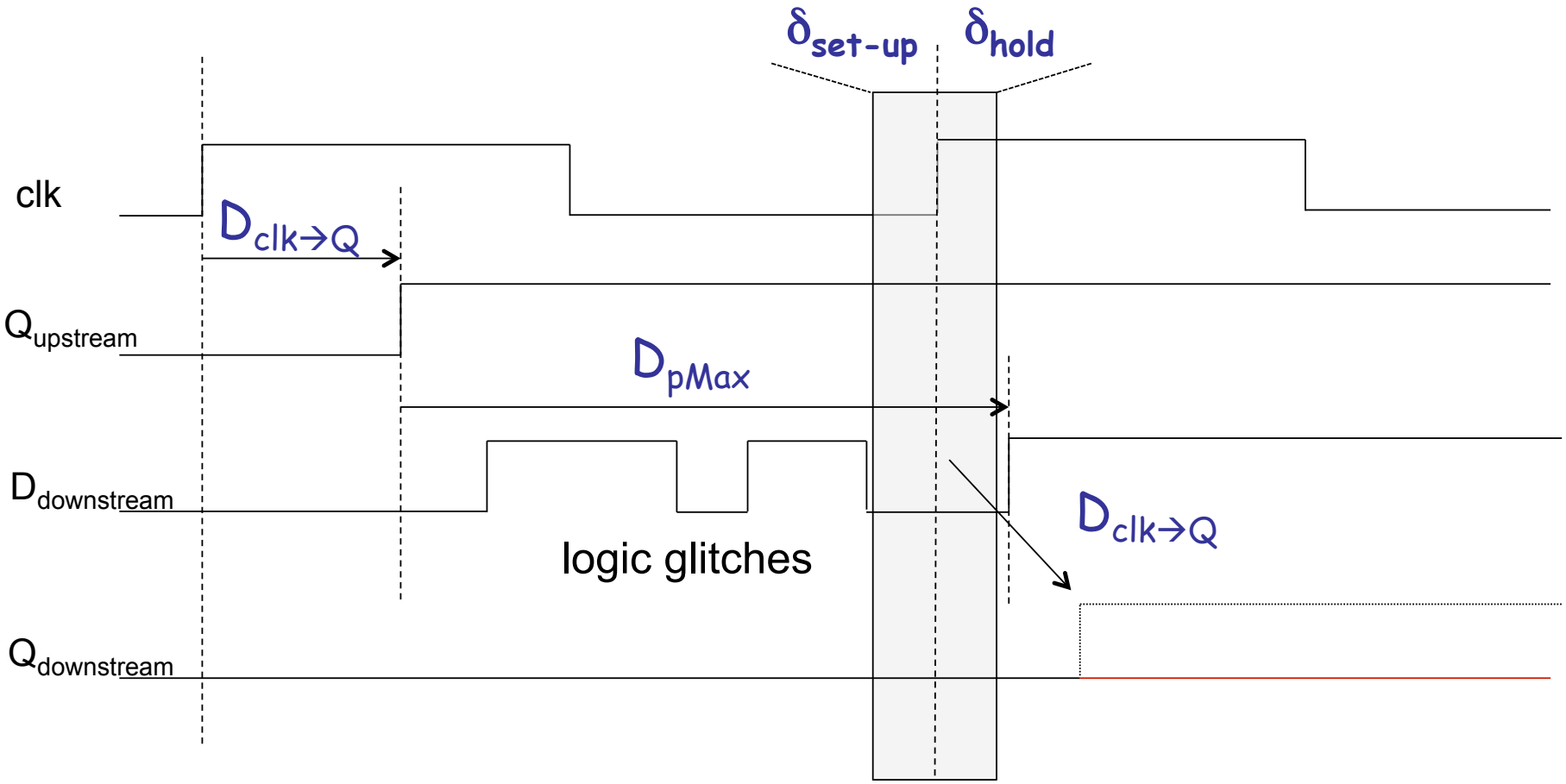


Setup time violation (i.e. timing constraint violation) :

⇒ metastability (non-deterministic)

Overclocking

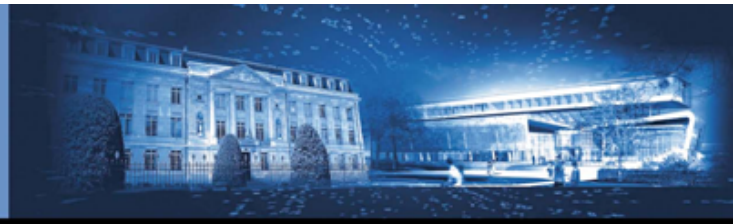


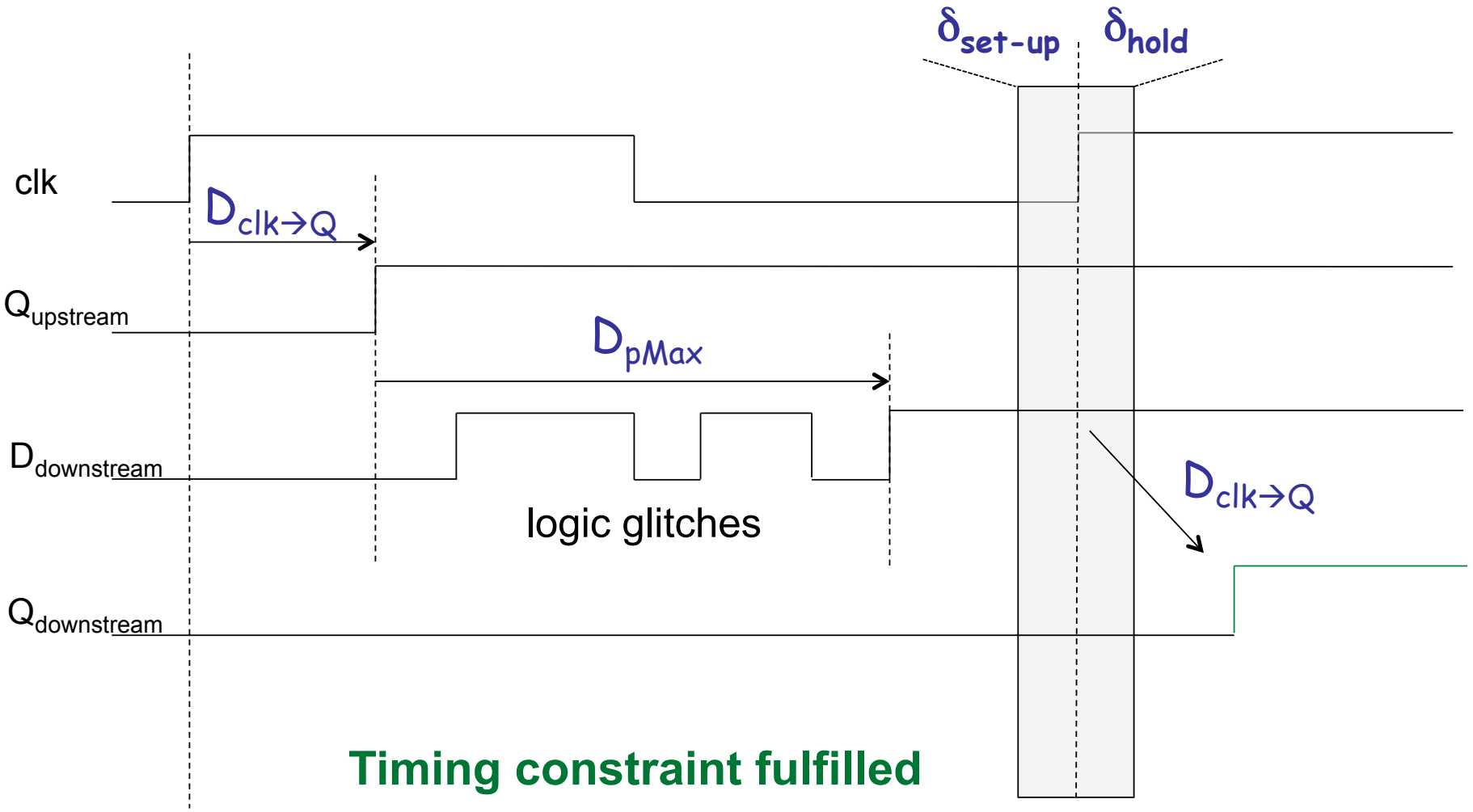


Timing constraint violation :

Early latching (deterministic)

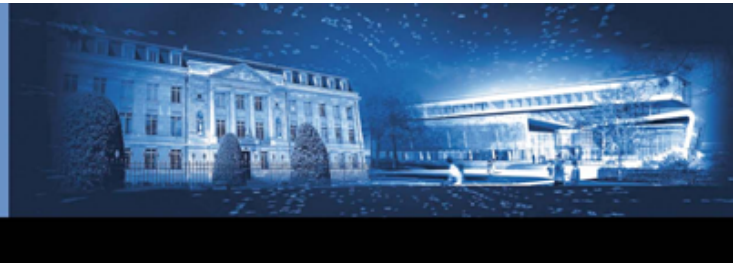
Underpowering/Overheating

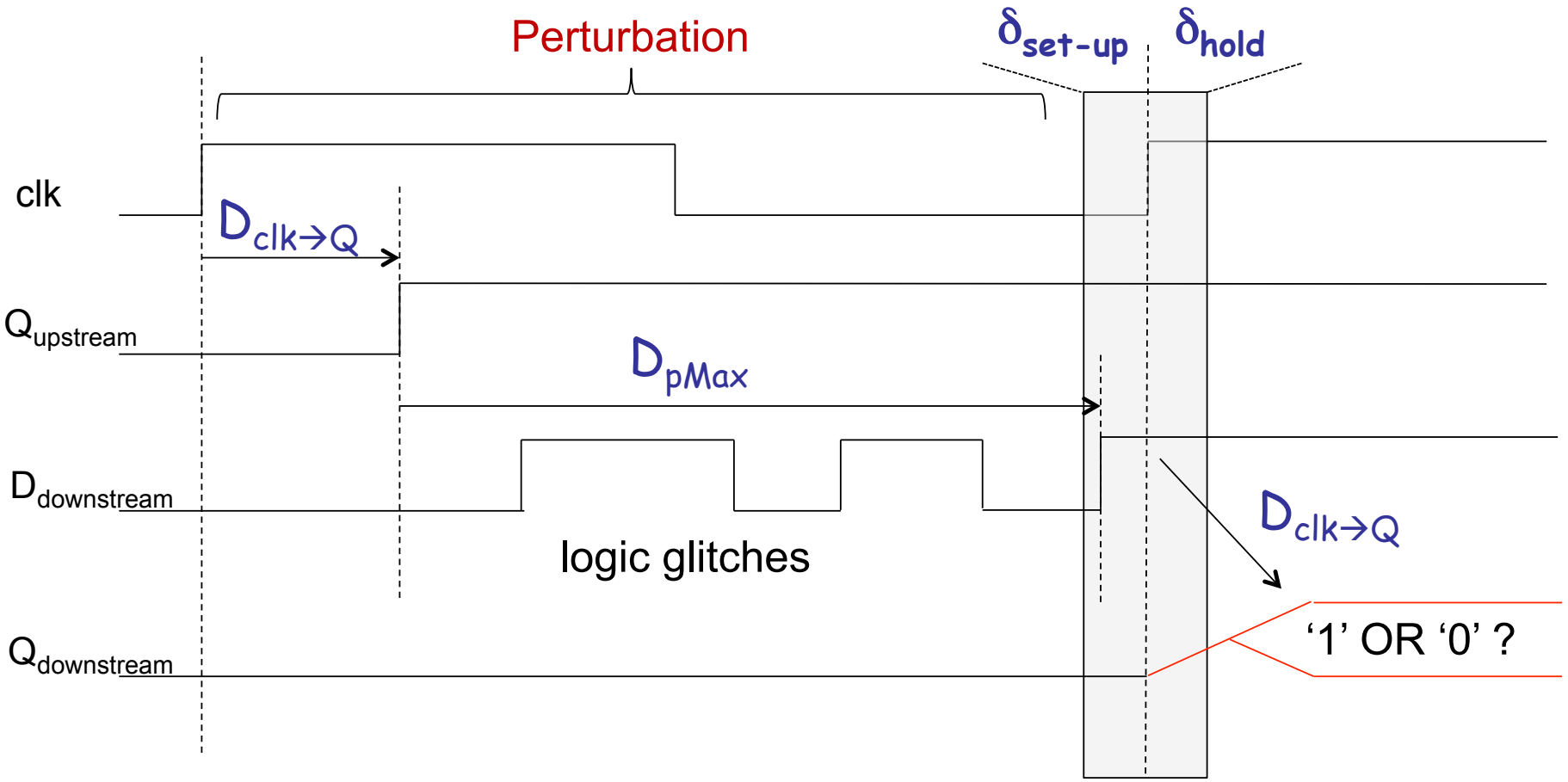




Timing constraint fulfilled

Underpowering/Overheating

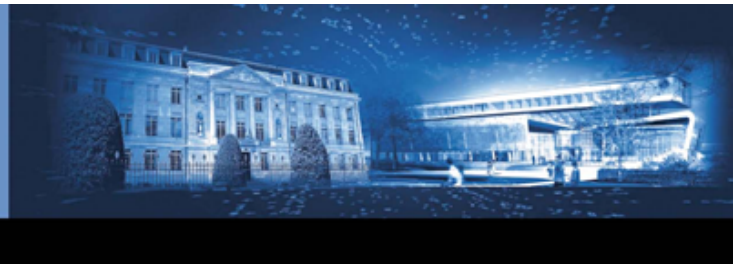


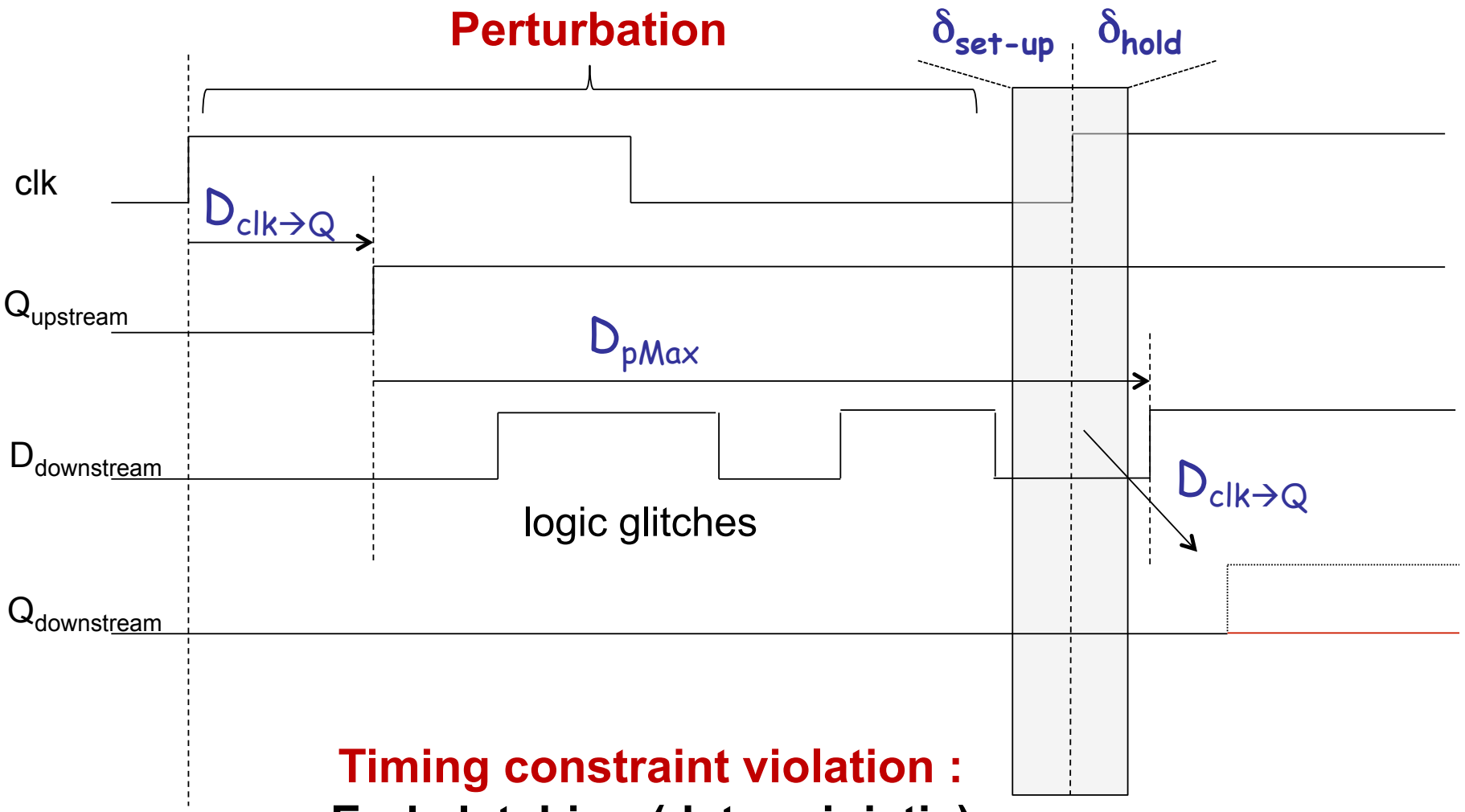


Setup time violation (i.e. timing constraint violation) :

⇒ metastability (non-deterministic)

Underpowering/Overheating



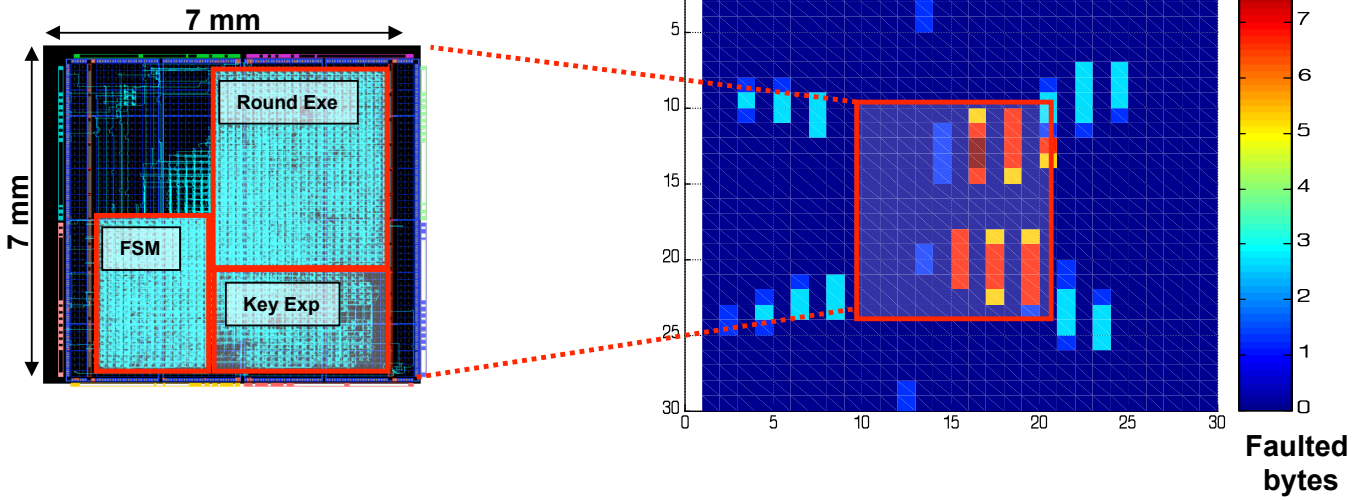


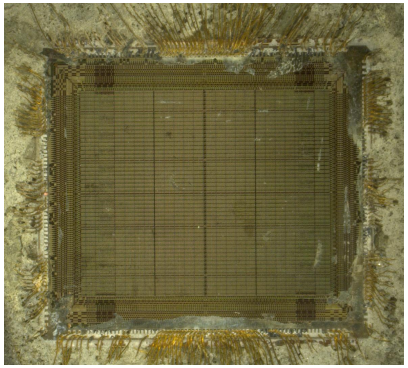
Timing constraint violation :

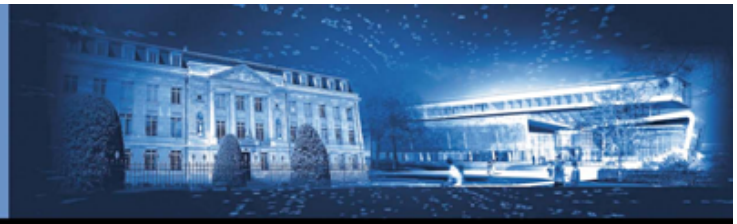
Early latching (deterministic)

Further work

EM pulse



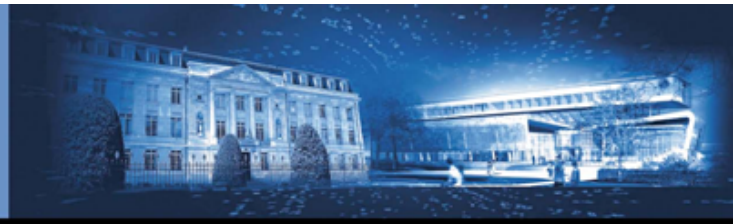




Context

- Many of our daily used electronic devices embed cryptographic features,
- Often targeted by malicious attackers,
- Indepth understanding of attack means is needed to protect properly these devices.

References



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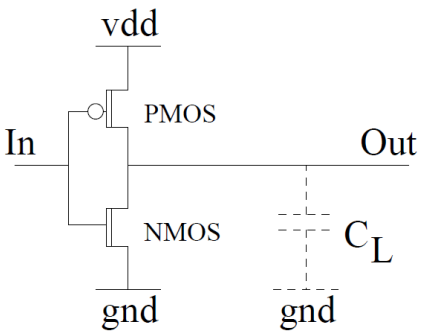
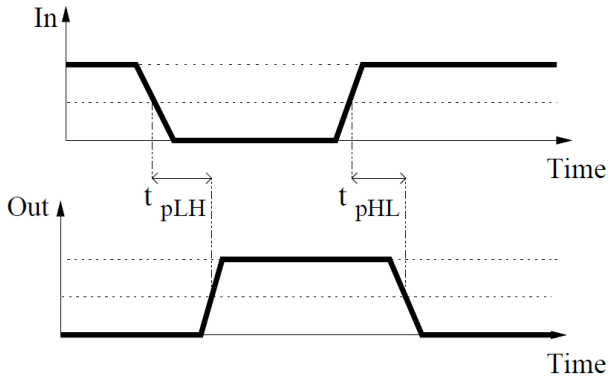
Timing constraints violation

Inverter :





$$t_{pLH} = \frac{C_L \left[\frac{2|V_{th,p}|}{V_{DD} - |V_{th,p}|} + \ln\left(3 - 4\frac{|V_{th,p}|}{V_{DD}}\right) \right]}{\mu_p C_{ox} \frac{W_p}{L_p} (V_{DD} - |V_{th,p}|)}$$

- Power Supply.

V_{DD} ↘ => t_{pLH} ↗

- Mobility :

temperature dependent.

T° ↗ => t_{pLH} ↗

(generally)