Building the electrical model of the Photoelectric Laser Stimulation of a PMOS transistor in 90nm technology

A Sarafianos, R Llido, O Gagliano, V Serradeil, M Lisart, V Goubier, Jean-Max Dutertre, A Tria, V Pouget, D Lewis

http://dx.doi.org/10.1016/j.microrel.2012.06.047

Building the electrical model of the Photoelectric Laser Stimulation of a PMOS transistor in 90nm technology

A. Sarafianos[a,b*], R. Llido[a,c], O. Gagliano[a], V. Serradeil[a], M. Lisart[a], V. Goubier[a], J.M. Dutertre[b], A. Tria[b], V. Pouget[c], D. Lewis[c]

[a] *STMicroelectronics, Avenue Célestin Coq 13790 Rousset, France*
[b] *Centre de Microélectronique de Provence - Georges Charpak 880 Avenue de Mimet 13541 Gardanne, France*
[c] *Université de Bordeaux 351 Cours de la Libération 33405, Talence, France*

Abstract

This paper presents the electrical model of a PMOS transistor in 90nm technology under 1064nm Photoelectric Laser Stimulation. The model was built and tuned from measurements made on test structures. It permits to simulate the effect of a continuous wave laser on a PMOS transistor by taking into account the laser's parameters (i.e. spot size and location, or power) and the PMOS' geometry and bias. It offers a significant gain of time by comparison with experiments and makes possible to build 3D photocurrent cartographies generated by the laser on the PMOS.

1. Introduction

Failure analysis (FA) methodologies make an extensive use of laser stimulation techniques. These techniques are very expensive and time consuming. In this paper, we present an electrical model of Photoelectric Laser Stimulation (PLS) of a PMOS transistor in 90nm technology. This electrical model makes it possible to simulate the response of a PMOS to PLS in a very small amount of time by comparison with real experiments on a laser equipment. Thus, the correct behaviour of a device under test may be predicted by simulation. It may serve as a "golden" reference to detect any defect by comparison and measurements. This approach permits a significant gain of time by reducing the need to use a laser source for characterization purposes. Obviously the obtained models are technology and layout dependent. Then, a new model has to be built for any technology improvement. Such models are intended to reduce the time passed on laser equipments.

This work presents the electrical model, (thanks to ELDO which is a SPICE simulator from Mentor Graphics [1]), of the photoelectric effect applied to a PMOS transistor in 90nm CMOS technology under backside continuous PLS. This model is valid for small laser power (~mW). In order to validate and correlate the model, measurements on PMOS transistors under laser illumination at a wavelength of 1064nm were performed with an I-phemos Hamamatsu equipment [2].

The novelty of the model presented in this paper is that it takes into accounts the laser's parameters (i.e. spot size and power), spatial parameters (i.e. the spot location and the PMOS' geometry), and the PMOS' bias. Therefore, the model is calibrated for each laser conditions (power, spot size, location, etc.) [3].

This article is organized as follows. Section 2 reports the behaviour under PLS of the two kinds of PN junctions encountered in PMOS transistors: P+/Nwell and Nwell/Psubstrate junctions. Measurements made on silicon permit to build an accurate electrical model. These models are used in turn to build a complete electrical model of a PMOS transistor under PLS as described in section 3. It offers the ability to draw 3D cartographies of PLS of PMOS for FA purposes as reported in section 4. Finally, our findings are summarized in the concluding section 5 with some perspectives.

2. Electrical modelling of the PN junctions found in PMOS transistors

In a PMOS transistor there are three PN junctions which are susceptible to give rise to a photoelectric effect if exposed to a laser beam (Drain/Nwell, source/Nwell, and Nwell/Psubstrate). Therefore to well model a PMOS transistor under laser illumination, it is first of all necessary to understand the phenomenon involved when a PN junction is stimulated by a photoelectric laser.

corresponding author: alexandre.sarafianos@st.com, fax: +(33) 442.688.729, phone: +(33) 442.688.536

2.1. PN junctions measurements under PLS

The Device Under Test (DUT) is a Pwell on Nwell junction embedded in a test structure of a STMicroelectronics 90nm technology. The test series were performed with a 20X objectives and a laser spot located in the middle of the diode and focused on the active zone. The laser power at the output of the chosen objective is adjustable between 0 and 41mW.

The I(V) characteristics depicted on figure 1 were obtained for various laser power according the aforementioned settings. A strong induced photocurrent was measured for the PN junction in reverse-biasing. The wide Space Charge Region of the junction in reverse bias explains that result. At the given power settings, any variation in the bias has no effect on the photocurrent provided it is maintained in reverse-biasing. However, when the diode is forward-biased (over its threshold voltage ~0.7V) the SCR is tightened and the induced photocurrent is almost negligible by comparison with the current flow in the diode [4].

In first approximation, and only with small laser power on this technology, it is possible to highlight the fact that in reverse mode the diode generates a constant photoelectric current independently of the voltage applied to its two electrodes.

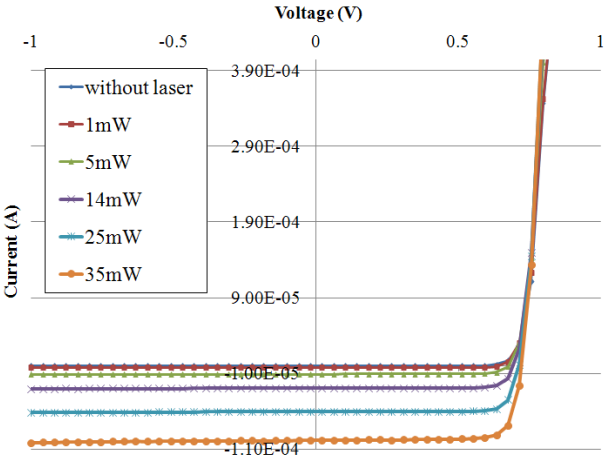

Fig. 1. I(V) characteristics of a junction Pwell on Nwell under PLS for different laser power.

Moreover, in reverse mode, the evolution of the photoelectric current generated in the diode versus the laser power is not linear. It is indeed possible to approximate it by a second order polynomial function presented in (1).

$$I_{laser} = 0.0323 * P_{laser}{}^{2} + 0.3335 * P_{laser} - 0.1624 \qquad (1)$$

Where I_{laser} is the current generated in the PN junction by the laser in Ampere and P_{laser} is the laser power in W/cm².

2.2. Study of the spatial dependence of the induced photocurrent

The distance between the laser spot and the PN junction has a strong impact on the value of the generated photocurrent. In the following, this effect is studied for both P+/Nwell and Nwell/Psubstrate diodes. That is why it is important to study this effect on P+/Nwell and Nwell/Psubstrate diodes.

When the laser beam is centered on the PN junction, the photocurrent is maximum, and when the laser moves outside the junction the value of the photocurrent deacreases.

2.1.1. Study of the P+/Nwell junction

In order to model the spatial dependence effect on a drain/bulk diode (P+/Nwell junction), a PMOS transistor with long channel (W=L=10µm) was used. The measurements were made with the drain at 1.2V, the bulk grounded, and the two other electrodes left floating. The laser spot was moved on a line from the center of the junction to a distance of 300µm. For each step, the photocurent was measured. This experiment was conducted for the three objectives of our laser I-phemos equipement (2.5X, 20X, and 50X) [2].The obtained photocurent versus distance curves are depicted on figure 2 after normalization according the maximum photocurrent (Iph2.5X, Iph20X, and Iph50X). Their shapes exhibit a Gaussian-like behaviour.

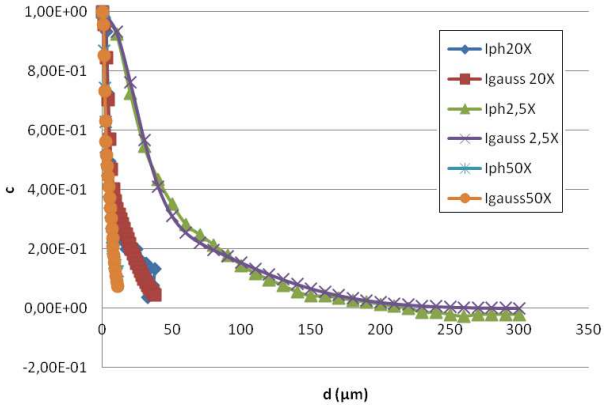

Fig. 2. *Spatial dependence of the induced photocurrent (measurements and models).*

It makes it possible to extract a mathematical model based on the sum of two Gaussian functions (2), where *d* is the distance between the spot and the junction expressed in µm:

$$\alpha_{gauss}(d) = a * \exp\left(-\frac{d^2}{c_1}\right) + b * \exp\left(-\frac{d^2}{c_2}\right) \qquad (2)$$

For each I-phemos objective, the coefficients a, b, c_1 and c_2 were found different (see Table I).

Table 1
Coefficients of the Gaussian function (2) for the different I-phemos objectives for the drain/bulk study.

Coefficient	2.5X	20X	50X
a	0.4	0.6	0.7
b	0.6	0.4	0.3
c_1	2.5	23.8	1000
c_2	55	654	15000

The three functions approximated mathematically (*Igauss2.5X*, *20X*, *50X*) are also plotted (See Fig. 2).

2.2.2. Study of the Nwell/Psubstrate junction

For the Nwell/Psubstrate junction, the same methodology was used than for the Drain/Bulk junction. The Gaussian profiles of the laser effect on silicon is not the same than for the drain/bulk junction. The main difference is due to the important area of the diode Nwell/Psubstrate. (20µm x 20µm). Table 2 presents the coefficient of equation (2) in order to model Gaussian effect of laser on Nwell/Psubstrate junction.

Table 2
Coefficients of the Gaussian function (2) for the different I-phemos objectives for the Nwell/Psubstrate junction study.

Coefficient	2.5X	20X	50X
a	0.5	0.6	0.7
b	0.5	0.4	0.3
c_1	2	1000	1500
c_2	48	15000	17000

Therefore wherever the laser beam is located on the studied device, the model is able to give the value of the photocurrent generated on the electrodes of the PMOS transistor.

2.3. Electrical model of a PN junction

In order to simulate a PN junction under PLS, the solution proposed in this paper is to define two sub circuits: *Subckt Iphp* to emulate the source and drain photocurrent generation, and *Subckt Iph_nw_psub* to simulate the laser effect on the diode Nwell/Psubstrate. These sub circuits contain a current source whose intensity value is defined for both by the parameter *Iph_val* (3):

$$Iph\_val = S * Ilaser * \alpha_{gauss} \quad (3)$$

Where S is the junction area in µm^2, I_{laser} is the value of the photocurrent generated on the PN junction (as defined in (1)) in Amper, and α_{gauss} the spatial dependency coefficient (cf. (2)). Note that α_{gauss} has different values for the two kind of diode (P+/Nwell and Nwell/Psubstrate).

The photocurrent generated on source and drain electrodes takes into account the value of the coefficient c which depends on the distance parameter d decided by the user for each junction of the PMOS, as noticed in equation (2). The coefficient a, b, c_1 and c_2 are those define in Table 1.

For the photocurrent generated on the diode Nwell/Psubstrate the same process is used. But, this time the simulator uses the parameter from Table 2.

3. Electrical model of a PMOS transistor under PLS

3.1. Building the electrical model of the PMOS under PLS

After the calibration step of the two different sub-circuit (*Iphp* and *Iph_nw_psub*) it is possible to model a 90nm technology PMOS transistor under PLS on the basis of manufacturer technological MOS models. On the four MOS electrodes, two sub circuits which model the P+/Nwell junctions under PLS (Sub circuits *Iphp*) are called by the main program. In the same way the sub circuit *Iph_nw-Psub* is called. (see Fig. 3).

When the user calls these sub circuits in the main netlist, for each junction he has to inform the value *S* (area of the junction), and *d* (shortest distance between the centre of the laser spot to the edge of the junction).

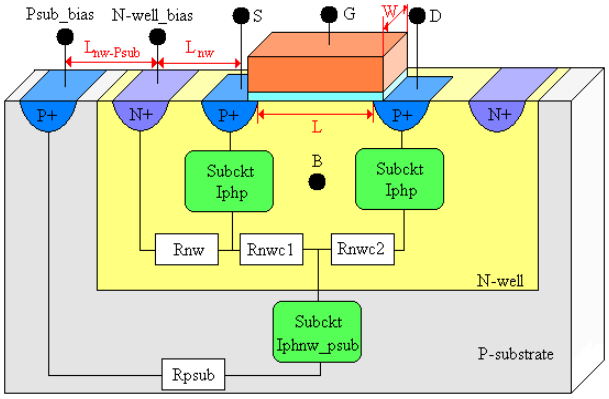

Fig 3. ELDO model of the PMOS under PLS.

Values of the 3 resistances of the model are defined as following (with geometrical parameters in µm defined on figure 3):

$$R_{nwc1} = R_{nwc2} = R_{nw}^{\square} * \frac{L}{2W} \quad (5)$$

$$R_{nw} = R_{nw}^{\square} * \frac{L_{nw}}{W} \quad (6)$$

$$R_{psub} = R_{Psub}^{\square} * \frac{\left(L_{nw} + L_{nw-Psub} + \frac{L}{2}\right)}{W} \quad (7)$$

Where $R_{nw}^{\square}$ and $R_{psub}^{\square}$ are the value of the resistance of each different type of silicon for one square.

Therefore the model takes into account the diodes area, the different possible places of the laser beam on the device, and different PMOS' bias chosen by the user.

3.2. Static laser positioning

This electrical model is able to simulate the effect of PLS for the different states of the PMOS transistor (On/Off). Graphs Fig. 5a and 5b highlight the good correlation between ELDO simulation and measurements on a turned OFF PMOS transistor W=10µm/L=0.09µm (See Fig. 5a) and a turned ON PMOS W=10µm/L=1.2µm (See fig. 5b), when the laser beam is parked in the middle of the PMOS transistor.

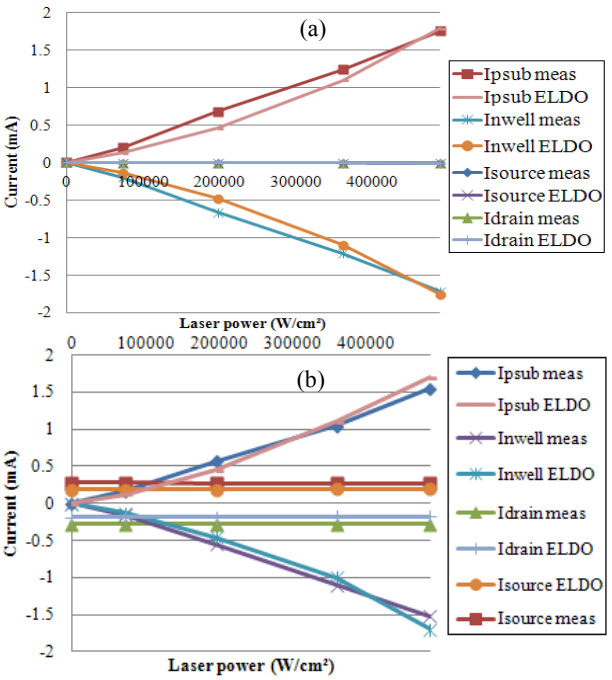

Fig. 5. ELDO simulation for a spot parked in the center of the device, at different laser power, with a spot size of 3.25µm.
(a) PMOS transistor W=10µm/L=0.09µm turned OFF
(b) PMOS transistor W=10 µm/L=1.2µm turned ON

4. Current cartographies

In this section, it is proposed to draw 3D current cartographies (extracted from the ELDO simulator) of photocurrents generated on a PMOS transistor W=L=10µm [5]. The user has the possibility to define the meshing density of cartographies thanks to a parameter called *stepXY*. This parameter is defined in function of the parameter distance *d*. It is also possible to extract 3D cartographies of photocurrents generated by the three PN junctions of a PMOS.

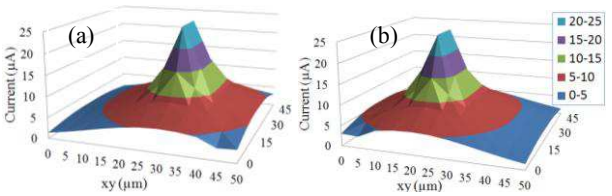

Fig. 6. 3D cartography extracted from ELDO of:
(a) the source under PLS.
(b) the drain under PLS.

The 3D cartographies of the photocurrent generated in the two P+/Nwell junctions highlight the Gaussian shape of the laser amplitude versus the spot location (See Fig. 6).

Due to the important area of the Nwell, the 3D current cartography extracted from the ELDO simulation, (and confirmed by measures) does not have the same profile. The value of the maximal photocurrent is higher (1.45mA) (See Fig. 7).

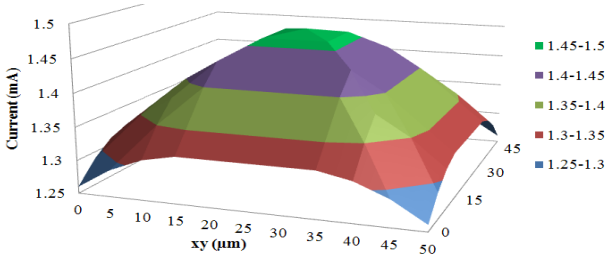

Fig. 7. 3D cartography of the photoelectric contribution of the Psubstrate under PLS extracted from ELDO.

5. Conclusion and perspectives

The electrical ELDO simulation (based on SPICE language) of the interaction between laser and silicon on a PMOS transistor in 90nm technology seems to be an extremely reliable, fast and also economical tool. In failure analysis it could have a great utility in order to compare the simulated response of a golden circuit under PLS with actual measurements. We have studied in a first place the modelling of PMOS transistors under PLS, because it is more complex to build than for NMOS (hence, a third PN junction between the N and P wells is encountered in PMOS). The validity of our approach is assessed by the very good correlation obtained between simulations and measurements. This work will be extended to NMOS transistors. Therefore, as a perspective, it will permit us to simulate the behaviour under PLS of complex logic gates made of PMOS and NMOS transistors.

References

[1] ELDO user's Manual – Software Version 6.6_1 Release 2005.3 – Mentor Graphics user's manual, 2005.

[2] Inverted Emission Microscope iPHEMOS Series Hamamatsu, « commercial brochure », 2011.

[3] K. Sanchez, R. Deplats, F. Beaudoin, P. Perdu, D. Lewis, P. Vedagarbha, and G. Woods, "Delay variation mapping induced by dynamic laser stimulation", Proceedings of 43rd IEEE International Reliability Physics Symposium (IRPS), vol. issue pp. 305-311, 2005

[4] A. Glowacki, Ph.D Thesis, "Expanding the scope of laser stimulation techniques for functional analysis and reliability of semiconductor devices by in-depth investigation of the optical interaction with the devices", Berlin University of Technology, 2010.

[5] R. Llido, J. Gomez, V. Goubier, G. Haller, V. Pouget, D. Lewis, "Improving defect localization techniques with laser beam with specific analysis and set-up modules", Proceedings of IEEE International Reliability Physics Symposium (IRPS), in press.