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Characterization and TCAD Simulation of 90nm Technology PMOS Transistor Under Continuous Photoelectric Laser Stimulation for Failure Analysis Improvement

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Abstract

This study responds to our need to optimize failure analysis methodologies based on laser/silicon interactions, using the functional response of an integrated circuit to local laser stimulation. Thus it is mandatory to understand the behavior of elementary devices under laser stimulation, in order to model and anticipate the behavior of more complex circuits. This paper characterizes and analyses effects induced by a static photoelectric laser on a 90 nm technology PMOS transistor. Comparisons between currents induced in short or long channel transistors for both ON and OFF states are made. Experimental measurements are correlated to Finite Elements Modeling Technology Computer Aided Design (TCAD) analyses. These physical simulations give a physical insight of carriers generation and charge transport phenomena in the devices.

Introduction

While performing Photoelectric Laser Stimulation (PLS) with a 1064 nm wavelength laser electron-hole pairs are generated in silicon, since the laser energy is greater than the band gap energy of silicon. In electric-field free areas or silicon substrate these carriers will diffuse and recombine rapidly without any significant effect. However, inside Space Charge Regions (SCR) of PN junctions (such as Drain-Source/Nwell or Nwell/substrate junctions of a transistor), those electron-holes pairs will be separated by the internal electric field and an Optical Beam Induced Current (OBIC) will be generated [1].

Our purpose is to analyze complex circuits response to PLS. For that, elementary devices are studied first and then more and more complex ones. This work follows a previous investigation on the 90nm technology NMOS transistor [2 3]. We study in this paper the effects of static PLS on a 90 nm technology PMOS transistor, in function of its channel length and its state. Electrical measurements associated with Finite Element Modeling software are useful and completing tools in order to understand and characterize PLS impact. TCAD models the complex flow of semiconductor fabrication steps leading to detailed information on geometric shape and doping profile distribution of a semiconductor device in scope (like a MOS transistor). It also uses this information to predict characteristics of semiconductor devices leading to circuit simulation models as implemented in any circuit simulator like PSPICE [4]. Three-dimensional simulation is computationally intensive and requires very long simulation times. Thus, only two dimensional (2D) TCAD simulations have been considered. We assume that the third space dimension does not significantly affect the behavior of the fundamental mechanisms involved in the following results, as the third dimension of the device (width of the transistor) is taken long enough to neglect edge effects (W=10µm). Moreover, comparisons between simulations and measures will rather be qualitative than quantitative because TCAD simulations are used as an analysis tool of physical laws effects inside a structure, and should be accurately calibrated before any quantitative analysis.

In a first section, this paper presents experimental characterization of the effect of PLS on a PN junction, which is compared to TCAD simulations. Then, a detailed analysis of PLS impact on a PMOS transistor is presented in function of the substrate polarization.

P+/Nwell junction

In this section, PLS impact on a P+/Nwell junction, already characterized in [5 6] is studied and compared to TCAD simulation in order to validate the models used on a well known case.

Experimental characterization

The Device Under Test (DUT) is embedded in a 90nm technology test structure and its surface is about 200µm². The experimentation was realized on an i-Phemos Hamamatsu system. The laser spot was positioned in the center of the junction and laser power was adjustable below 100mW. Current-voltage (I-V) characteristic was measured for different laser power, and presented on Figure 1. When the PN junction is reverse-biased under 0.6V, the photocurrent is almost constant independently of applied voltage since the SCR width does not vary significantly. The induced photocurrent is higher than the junction reverse leakage and depends on laser power. Then, when applied voltage raises over 0.6V, the SCR width starts to decrease and consequently the amount of induced photocurrent is also reduced. When the applied voltage reaches diode built-in potential (black cross on Figure 1), the SCR decreases, the induced photocurrent is therefore reduced and becomes negligible with respect to the junction forward current. Moreover, the so far negligible resistances of the P and N-type regions start to play a significant role in forward mode and get reduced under the illumination, which leads to a current increase with laser intensity.

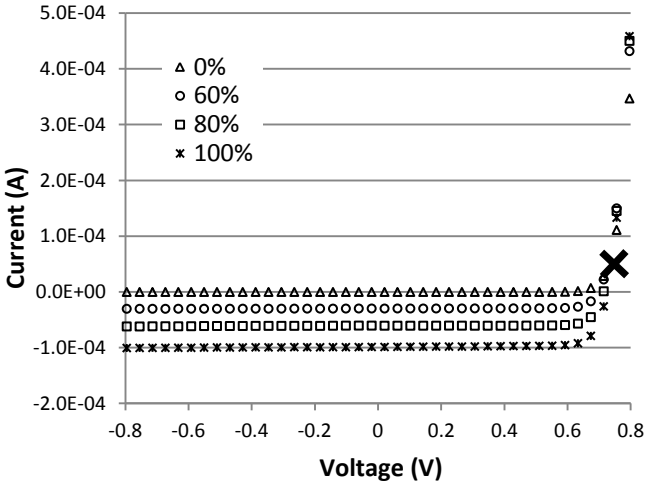

Figure 1. Measured I-V curve of P+/Nwell junction vs. laser power.

TCAD simulations

The goal of this simulation was to reproduce the photocurrent induced in the SCR of the device. In this work, Synopsys simulation tools are used and especially Sentaurus Device Editor (SDE) for grid generation and SDevice for device simulation. Sentaurus Process tool has been used to generate structures, reproducing all process steps used to build the devices. The simulated device is a Drain/Substrate (or Source/Substrate) junction obtained removing the gate and taking half of a PMOS transistor (Figure 2). Thus a single structure is generated and information about phenomena taking place into the transistor's junctions is obtained.

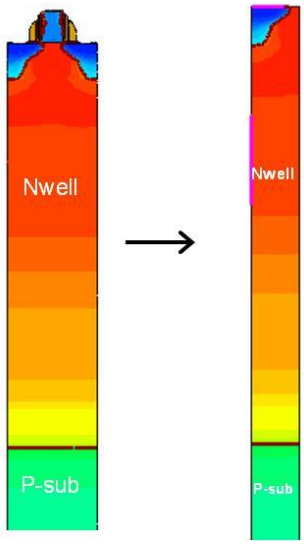

Figure 2. Structure used for junctions TCAD simulations.

I-V characteristics of the junction are simulated in function of the intensity (from 100 W.cm^{-2} to 500 W.cm^{-2}) of the 1064 nm smooth wave simulator (Figure 3). Results are correlated to measurements, currents levels are not identical to measurements because TCAD simulator is not calibrated to fit silicon results, it is only used to have trends.

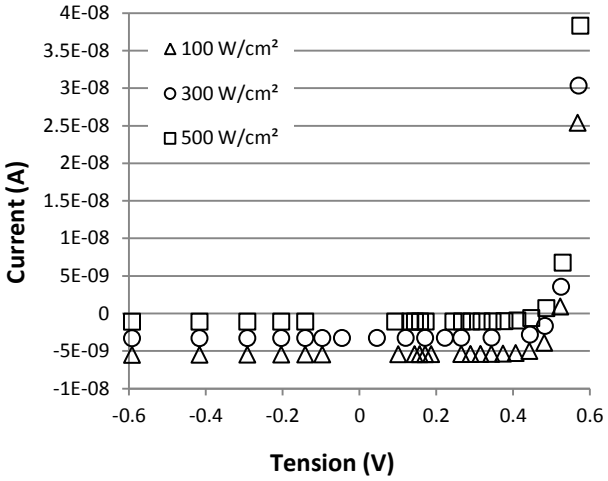

Figure 3. Simulated I-V curve of P+/Nwell junction vs. laser power.

Correlation of measurement and simulation

The same trends are obtained by experiments and by TCAD simulations: under photoelectric stimulation (1064 nm) a reverse-biased junction can be modeled by a current source, and the quantity of photocurrent does not significantly depend on the applied reverse voltage (valid for this technology).

Although junctions used for measurements and simulations are different in terms of geometry, the purpose of this study is to have a qualitative comparison (current trends) rather than a quantitative comparison (current amplitudes) between

experimental measurements and simulations. The aim was to validate simulation models on basic devices already studied, in order to simulate after that with confidence the effect of PLS on a more complicated component: a PMOS transistor.

PMOS transistor study

The effect of pulsed PLS on transistors has already been analyzed [7 8]. However, we aspire at understanding effects of static PLS on a PMOS transistor which can help us to interpret OBIC or LIVA cartography obtained in the field of a failure analysis. DUT are embedded in a 90 nm technology test structure and the laser power is adjustable below 100mW. For each study, the laser spot is positioned in the center of the transistor and current of each electrode is measured in function of the laser power [9]. In case of a PMOS transistor study, two cases must be investigated: when the p-substrate is floating and grounded.

Floating p-substrate

Long channel transistor

OFF state: A 10µm x 10µm PMOS transistor is biased as follows: Gate, Source and Nwell are biased at 1.2V and the Drain is grounded. Evolution of these four electrodes currents in function of the laser power is given in Figure 4. Obviously the gate current is always equal to zero. The current conservation law is respected since the sum of all currents is always equal to zero. Moreover, the same quantity of current is approximately generated in Drain/Substrate and Source/substrate junctions.

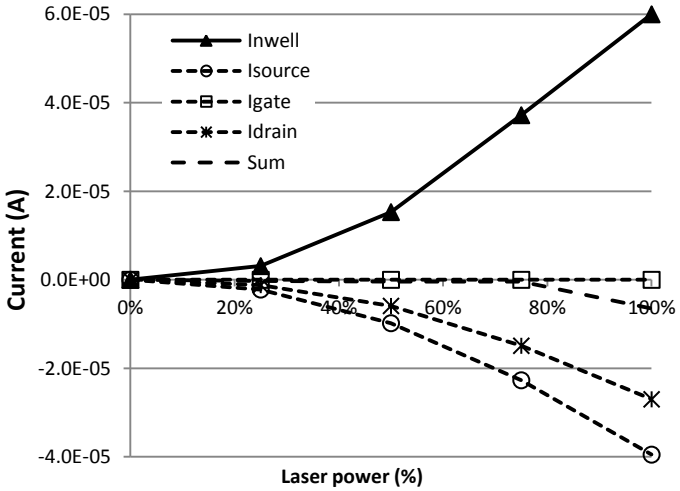

Figure 4. Long channel transistor currents vs. laser power (transistor in OFF state).

ON state: A 10µm x 10µm PMOS transistor is biased as follows: Gate and Drain are grounded; Source and Nwell are biased at 1.2V. Evolution of these four electrodes currents in function of the laser power is presented in Figure 5, and the conclusion is the same than in OFF state. Moreover, $|I_{source}|$ decreases since the starting up in conduction of the channel leads an additional current which opposes to the circulation of Source photocurrent. On the other hand, $|I_{drain}|$ increases because it comes to be added to the normal circulation of electrons in the channel (due to its starting in conduction). Finally, the same quantity of photocurrent is induced in the transistor in both ON and OFF states (Figure 6): approximately 30 µA in Source-Nwell or Drain-Nwell junctions and 65 µA in Nwell-Psubstrate junction (at maximum laser power).

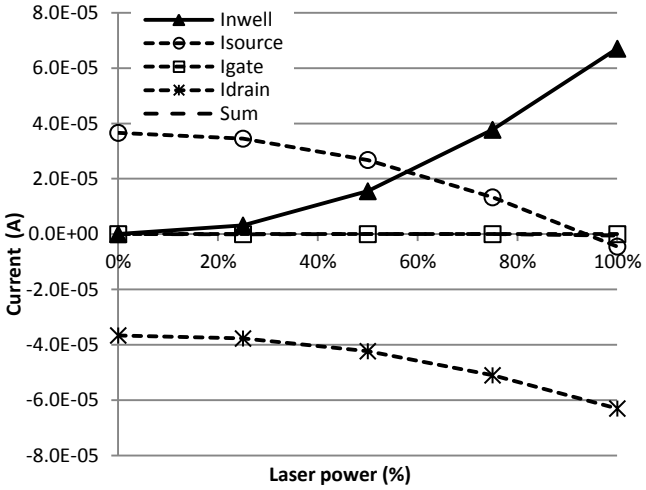

Figure 5. Long channel transistor currents vs. laser power (transistor in ON state).

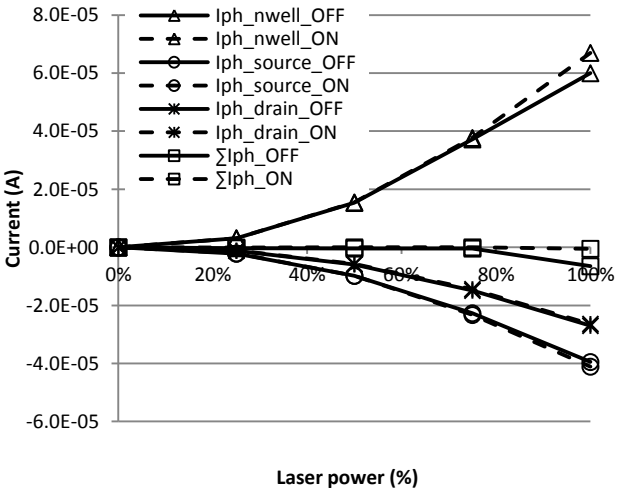

Figure 6. Long channel transistor photocurrent generation difference between OFF and ON states (in this case subtraction between the current values obtained with and without laser stimulation).

In conclusion, the effect of PLS is the same whether the long channel PMOS transistor is in OFF or ON state: its conduction is only slightly increased, and leakage currents are induced. This result is identical to the one obtained during the study of an NMOS transistor [2]. Consequently the effect of PLS is identical for both long channel NMOS and PMOS (with floating substrate) transistors.

Short channel transistor

OFF state: A 10µm x 0.09µm PMOS transistor is used. Evolution of electrodes currents in function of the laser power is presented in Figure 7. The quantity of photocurrent induced is approximately three times smaller than in the long channel transistor case (for example $I_{Drain\text{-}short\ channel}$= -8.1µA and $I_{Drain\text{-}long\ channel}$= -27µA).

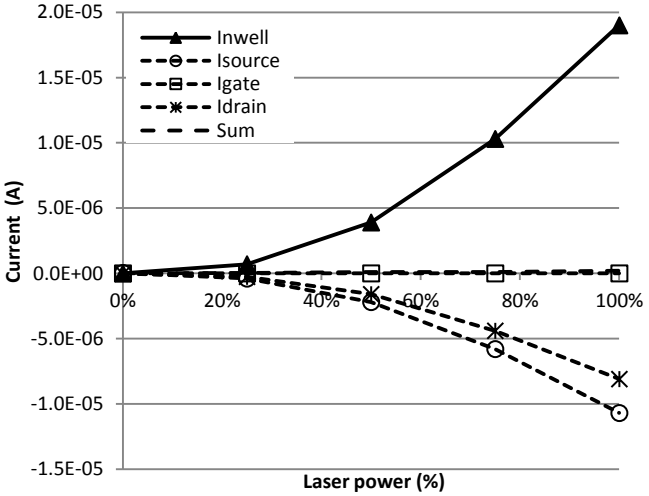

Figure 7. Short channel transistor currents vs. laser power (transistor in OFF state).

ON state: A 10µm x 0.09µm PMOS transistor is used. The current flow through these four electrodes as a function of the laser power is depicted on Figure 8. Contrary to the long channel transistor, the effect of laser stimulation is not visible even at maximum laser power. Indeed, current amplitudes measured when this short channel transistor is turned on are very important (approximately 2.7 mA for Source and Drain) compared to the quantity of photocurrent generated (about 20 µA), so the effect of PLS is negligible. Indeed, Drain current (at fixed V_{Gate}) varies proportionally to 1/L, that's why effect of PLS can be observed in ON state on a long channel transistor but not on a short channel one. A more detailed study on transistor length dimension variation is proposed in the following part.

These results are identical to those obtained during the NMOS transistor study [2]. In conclusion, the effect of PLS is the same on both short channel NMOS or PMOS (with floating substrate) transistors.

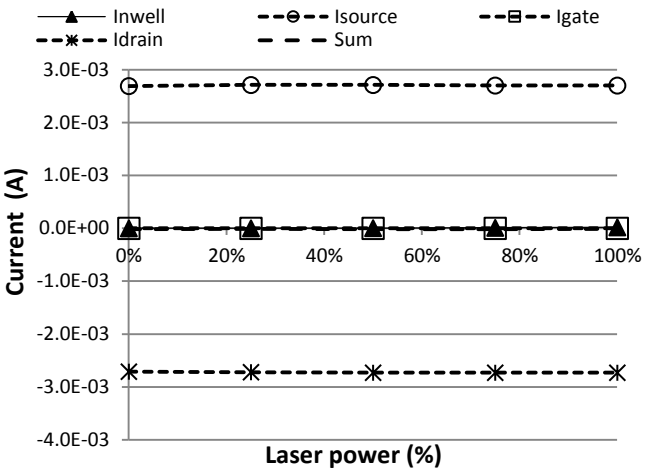

Figure 8. Short channel transistor currents vs. laser power (transistor in ON state).

Effect of transistor length variation

The previous part highlights the fact that in OFF state the quantity of induced photocurrent is three times smaller in case of a short channel. This point is investigated in this section through the study of the transistor gate length variation. Current values are measured at maximum laser power for different lengths (0.09µm, 0.1µm, 0.24µm, 0.5µm, 1.2µm, 5µm and 10µm), results are illustrated in Figure 9 and show that photocurrents increase with the transistor length. Same results are obtained with TCAD simulation tool. In all cases (from L=0.09µm to 10µm) current conservation is verified, but the amount of induced photocurrent is smaller for small L values although transistor is in OFF state (V_{gate}=0V), width are identical (W=10µm), and Source/Drain junctions volumes are identical. The reason is the same as in the NMOS transistor case [2] : a part of the total photocurrent collected on Source and Drain contact is a contribution from the channel depletion region.

In conclusion, effect of PLS on a PMOS transistor with floating p-substrate is similar than on a NMOS transistor: it depends on its gate length and on the applied voltages, conditioning the existence and the size of depletion regions in the Source and the Drain, and eventually in the channel region where photocurrents are generated. However, the most realistic situation of the CMOS technologies is when the Substrate is biased to the potential of reference (ground). In that case, the behavior under PLS of the PMOS transistor is very different.

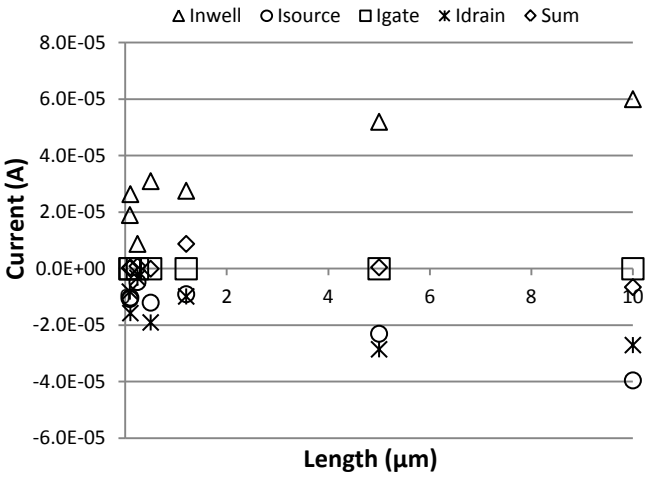

Figure 9. Photocurrent induced (at maximum laser power) vs.transistor lentgh (W=10µm).

P-substrate grounded

Long channel transistor

OFF state: The same experiment than in part A is done with the p-Substrate grounded. Results are presented in Figure 10. Gate current is always equal to zero, current conservation law is respected. When the p-Substrate is grounded, photocurrents collected at Drain and Source are small compared to the photocurrent induced in Nwell-Substrate junction. In this case we can consider that the laser stimulation has a dominating effect only on the Nwell-Substrate junction.

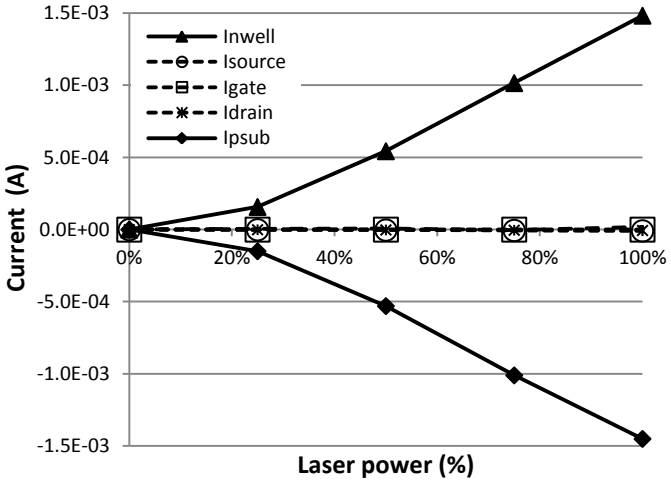

Figure 10. Long channel transistor currents vs. laser power (transistor in OFF state).

ON state: The same experiment than in part A is done with p-Substrate grounded. Results are presented in Figure 11, and the conclusion is the same than for a long channel transistor although Drain and Source current amplitudes are higher than in OFF state (since the channel is in conduction), but the effect of PLS remains smaller on them (even at maximum laser power). Finally, the same quantity of photocurrent is induced whether the transistor is in ON or OFF state (Figure 12).

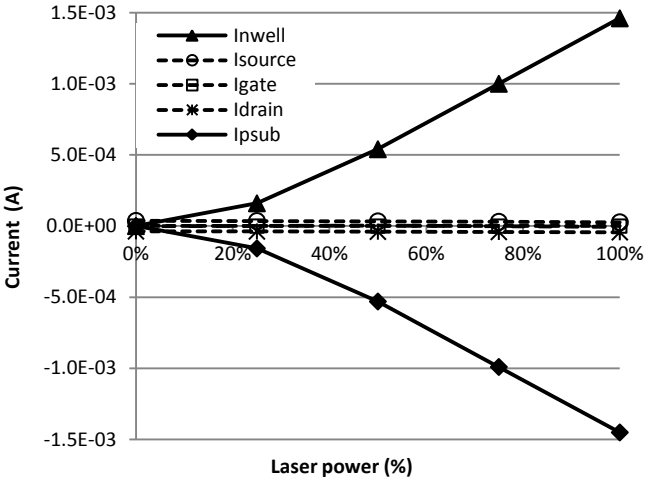

Figure 11. Long channel transistor currents in function of laser power (transistor in ON state).

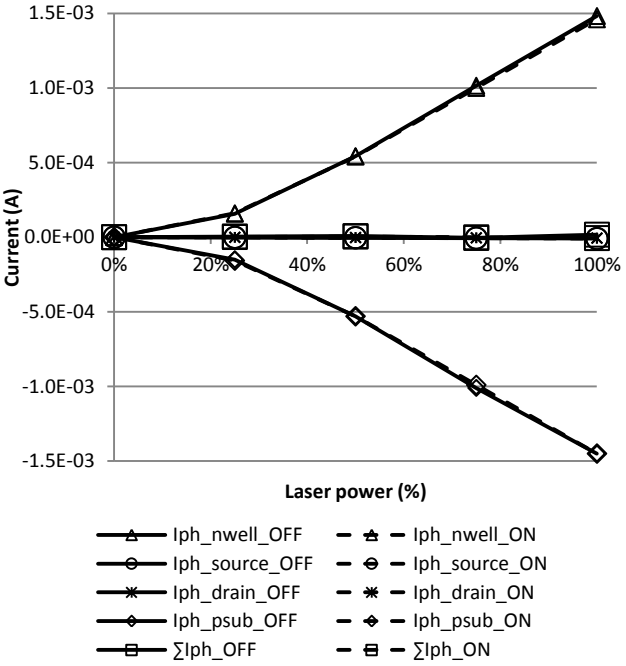

Figure 12. Long channel transistor photocurrent generation difference between OFF and ON states (in this case subtraction between the current values obtained with and without laser stimulation).

In conclusion, when the p-Substrate of a long channel PMOS transistor is grounded, effect of PLS is dominant on Nwell/Substrate junction compared to Source/Nwell and Drain/Nwell junctions. Two reasons explain this conclusion. First, if these three junctions had the same surface the Nwell photocurrent would be larger than the Source/Drain one because Nwell region doping is weaker (Figure 13),

consequently Nwell SCR width is bigger than the Source/Drain one. The fact that in a PMOS transistor the Nwell junction surface is more important stresses this point. Finally, if these three junctions had the same doping, photocurrent induced in the Nwell junction would be higher than in Source/Drain one because photocurrent is proportional to the surface : $I_{ph} = j_{ph}*S$ with S the junction surface. From both points of view the photocourant induced in Nwell junction is higher than in Source or Drain one.

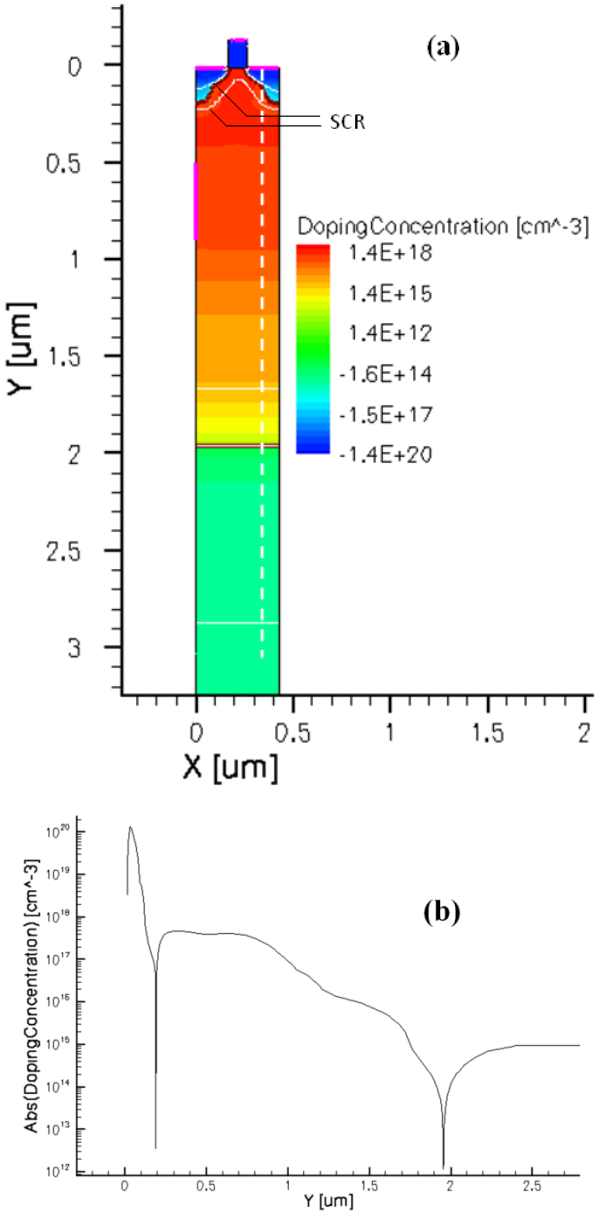

Figure 13. Doping concentration mapping and SCR displayed in white lines (a) and doping profile of the mapping along the white dashed line (b)

Short channel transistor

OFF state: The same experiment than in part A is realized on a 10µm x 1.2µm PMOS transistor with p-Substrate grounded. Results are presented in Figure 14 and the conclusion is the same as for a long channel transistor. Moreover, the same magnitude of current is measured as in the long channel transistor (for example, $I_{Source\text{-}short\ channel}$= -8.6µA and $I_{Source\text{-}long\ channel}$= -9µA, $I_{Nwell\text{-}short\ channel}$= 1.6mA and $I_{Nwell\text{-}long\ channel}$= 1.48mA).

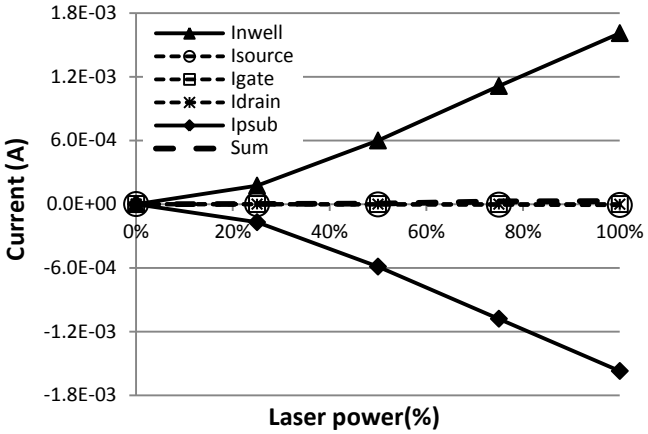

Figure 14. Short channel transistor currents in function of laser power (transistor in OFF state).

ON state: The same experiment than in part A is realized on a 10µm x 1.2µm PMOS transistor with p-Substrate grounded. Results are presented in Figure 15. As in the long channel case, Drain and Source current amplitudes are higher than in OFF state (since the channel is in conduction) but effect of PLS remains all the same negligible (even at maximum laser power).

In conclusion, the same magnitudes of photocurrent seem to be induced whether the transistor is short or long channel, in ON or OFF state.

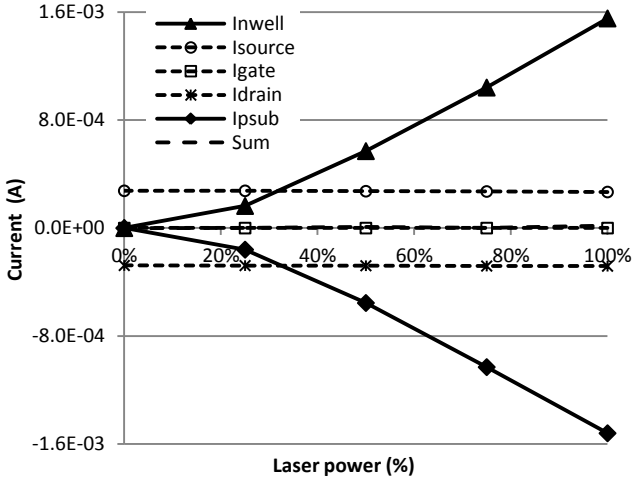

Figure 15. Short channel transistor currents in function of laser power (transistor in ON state).

Effect of transistor length variation

Photocurrents induced in Drain, Source, Nwell and p-Substrate in function of the transistor gate length when the transistor is in OFF state is studied in this paragraph. Currents values are measured at maximum laser power for different length dimensions (0.09µm, 1.2µm, 5µm and 10µm), results are presented in Figure 16 and show that photocurrent induced in each electrode slightly decrease between 0 and 2 µm, but remains constant over 2 µm. The same experiment is simulated with TCAD tool, results are presented in Figure 17. The trend of curves presented in Figure 16 and Figure 17 are different because in simulation the laser is simulated as a plane wave so there is the same power density over the whole structure. Whereas in measurements, the laser power density follows a Gaussian shape (see Figure 18). This means that in case of a very short channel transistor (L=0.09µm) source and drain are completely covered and centered in the laser spot, so they are irradiated with the maximum power and their photocurrent amplitudes are maximum. For short channel (between 0.1 and 2 µm), source and drain are at the edge of the laser spot, so source and drain photocurrent amplitudes are smaller than for smaller length values. When gate length is over 2µm, source and drain are outside the laser spot, so they are irradiated by the "feet" of the Gaussian and levels of photocurrents are smaller than for smaller gate length values, and keep almost constant.

In conclusion, when the p-substrate of a long channel PMOS transistor is grounded, the same quantity of photocurrent is theoretically induced whether the transistor is short or long channel. In practice, more photocurrent is induced in transistors owning gate length smaller than the laser spot diameter.

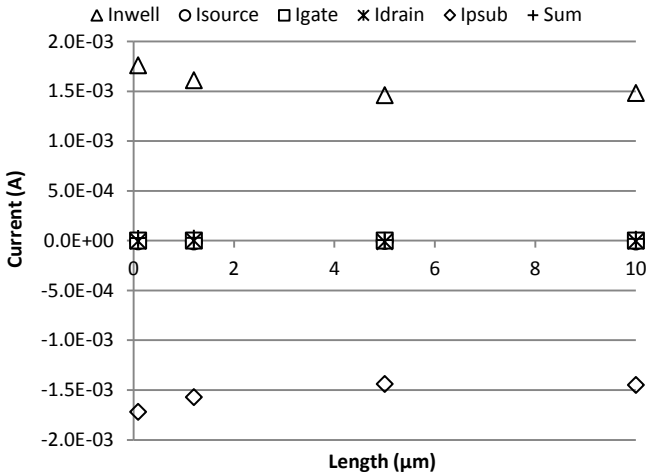

Figure 16. Measurements of photocurrent induced (at maximum laser power) in function of transistor lentgh (W=10µm).

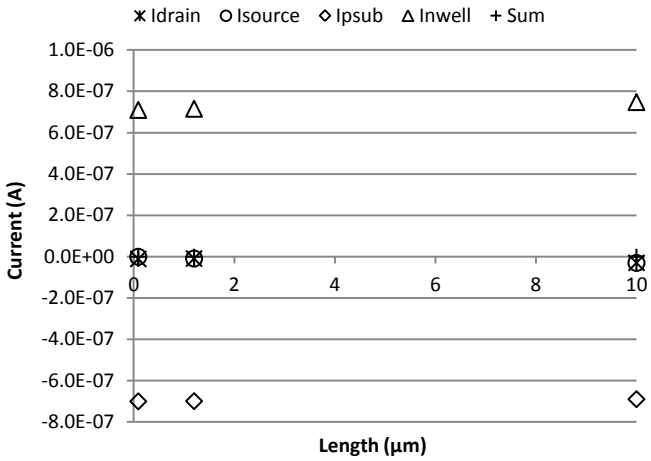

Figure 17. Simulation of photocurrent induced (at maximum laser power) in function of transistor lentgh (W=10µm).

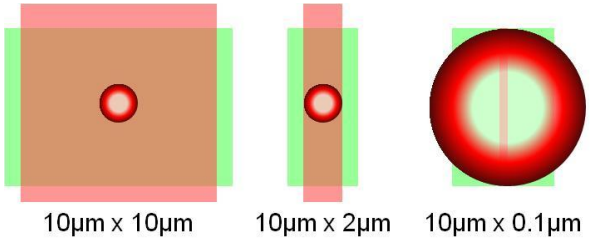

Figure 18. Laser spot size with respect to the gate length.

Conclusions

Effects of PLS on a 90 nm PMOS transistor have been investigated. Comparisons between photocurrents induced in case of short or long channel, or turned ON or OFF transistor are presented. Moreover, if the p-Substrate is floating, PMOS transistor behavior is equivalent to that of NMOS transistor.

This study gives the possibility to optimize failure analysis methodologies. Indeed, it reveals that static PLS induces non negligible leakages in a transistor (several micro amps in a single transistor) which explains why OBIC cartographies are difficult to interpret. Moreover, PLS does not bring enough energy to make a transistor change its state since in static the density of induced carriers is not important enough. This confirms that OBIC technique cannot be implemented such as OBIRCh [10 11] one and should rather be used in a dynamic approach [12]. This way, in presence of defects or if the product is in a state in limit of functionality, the very weak electric variations led by the laser stimulation will be able to modify the functionality of the integrated circuit, allowing the localization of sensitive zones. It will be possible to localize for example sources of Latch-Up triggering [13], or advance/delay of CMOS gates[14 15]. Finally, based on this study we developed an ELDO model (based on SPICE language) of a PMOS transistor submitted to PLS, that fit very well measurements. It will be useful in case of PLS of

complex circuit to predict results and compare them with simulation [16].

Future work will characterize PLS effect on simple logic gates or MOS inverter under PLS. The test with a pulsed laser will also be conducted to explore higher laser energy ranges [17].

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