Building the electrical model of the pulsed photoelectric laser stimulation of an NMOS transistor in 90nm technology

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Abstract

This paper presents the electrical model of an NMOS transistor in 90nm technology under 1064nm Photoelectric Laser Stimulation. The model was built and tuned from measurements made on test structures and from the results of physical simulation using Finite Element Modeling (TCAD). The latter is a useful tool in order to understand and correlate the effects seen by measurement by given a physical insight of carrier generation and transport in devices. This electrical model enables to simulate the effect of a continuous laser wave on an NMOS transistor by taking into account the laser's parameters (i.e. spot size and power), spatial parameters (i.e. the spot location and the NMOS' geometry) and the NMOS' bias. It offers a significant gain of time for experiment processes and makes it possible to build 3D photocurrent cartographies generated by the laser on the NMOS, in order to predict its response independently of the laser beam location.

Introduction

In the photoelectric effect, electrons are emitted from silicon as a consequence of their absorption of energy from light. Failure analysis (FA) methodologies make an extensive use of laser stimulation techniques. In this paper, we present an electrical model of the Photoelectric Laser Stimulation (PLS) of an NMOS transistor in 90nm technology. This electrical model makes it possible to simulate the response of an NMOS transistor to PLS in a very small amount of calculation time by comparison with real experiments on a laser equipment, or TCAD simulations. Thus, the correct behaviour of a device under test may be predicted by simulation. It may serve as a "golden" reference to detect any defect by comparison and measurements. Obviously the obtained models are technology and layout dependent. Thus, a new model has to be built for any technology improvement. Such models are intended to reduce the time passed on laser equipments.

This work presents the electrical model (thanks to ELDO, the SPICE simulator from Mentor Graphics [1]), of the photoelectric effect applied to an NMOS transistor in 90nm CMOS technology under backside continuous PLS. This model is valid for small laser power (from 0 to 100mW). In order to validate and correlate the model, measurements on NMOS transistors under laser illumination at a wavelength of 1064nm were performed with an I-phemos Hamamatsu equipment [2].

Moreover TCAD analyses are needed, in order to understand better the phenomenon involved when an NMOS transistor is under PLS. TCAD takes into account the complex flow of semiconductor fabrication steps leading to detailed information on geometric shape and doping profile distribution of a semiconductor device in scope (like a MOS transistor) [3] to model its behaviour. Three-dimensional simulation is computationally intensive and requires very long simulation times. Thus, only two dimensional (2D) TCAD simulations have been considered in this paper. We assume that the third space dimension does not significantly affect the behaviour of the fundamental mechanisms involved in the following results, as the third dimension of the device (width of the transistor) is taken as long enough to neglect edge effects (W=10μm). The laser waves used in all TCAD simulations are in every case, a plane wave which illuminates all the backside of devices.

Moreover, comparisons between measures and simulations will rather be qualitative than quantitative because TCAD simulations are first used as an analysis tool of physical laws effects inside a structure, and should be accurately calibrated before any quantitative analysis. Electrical measurements associated with Finite Element Modeling software are the tools necessary to understand and model PLS impact on NMOS transistor.

The novelty of the model presented in this paper is that it takes into accounts the laser's parameters (i.e. spot size and power), spatial parameters (i.e. the spot location and the NMOS' geometry), and the NMOS' bias. Therefore, the model is calibrated for each laser conditions (power, spot size, location, etc.)

This article is organized as follows. Section 2 reports the behaviour under PLS of PN junctions encountered in NMOS transistors: N+/Psubstrate junctions. Measurements made on silicon and TCAD simulations permit to build an accurate electrical model. This model is used in turn to build a complete electrical model of an NMOS transistor under PLS, with

comparison and measurements for different laser and NMOS parameters as described in section 3. This model offers the ability to draw 3D cartographies of NMOS under PLS for FA purposes as reported in section 4. Finally, our findings are summarized in the concluding section 5 with some perspectives.

Electrical modeling of the PN junction found in an NMOS transistor

In an NMOS transistor there are mainly two PN junctions which give rise to a photoelectric effect if exposed to a laser beam (Drain/Psubstrate and Source/Psubstrate). Therefore a first step toward building the electrical model of NMOS transistors under PLS is the study and modeling of PN junctions under laser illumination.

PN junctions measurements under PLS

The Device Under Test (DUT) is an N+ on Psubstrate junction embedded in a test structure of a STMicroelectronics 90nm technology. The test series was performed with a 20X objective and a laser spot located in the middle of the diode focused on the active zone. The laser power at the output of the chosen objective was adjustable between 0 and below ~100mW. The main characteristics of the experiment are presented on figure 1. The red spot represents the location of the laser beam on the diode layout.
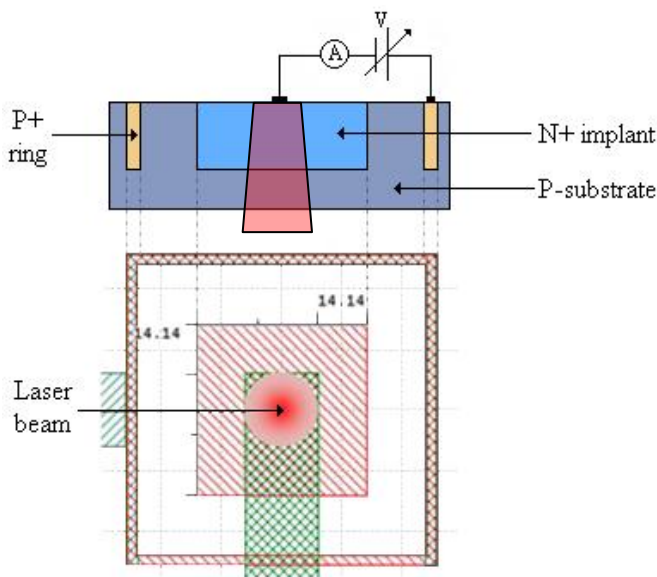

Figure 1: N+ on Psubstrate junction.

The I(V) characteristics depicted on figure 2 were obtained for various laser power according the aforementioned settings. A strong induced photocurrent was measured for the PN junction in reverse-biasing. The wide Space Charge Region (SCR) of the junction in reverse bias explains that result. At the given power settings, any variation in the bias has no effect on the photocurrent provided it is maintained in reverse-biasing.

However, when the diode is forward-biased (over its threshold voltage ~0.7V) the SCR is tightened and the induced photocurrent is almost negligible by comparison with the current flow in the diode [4].
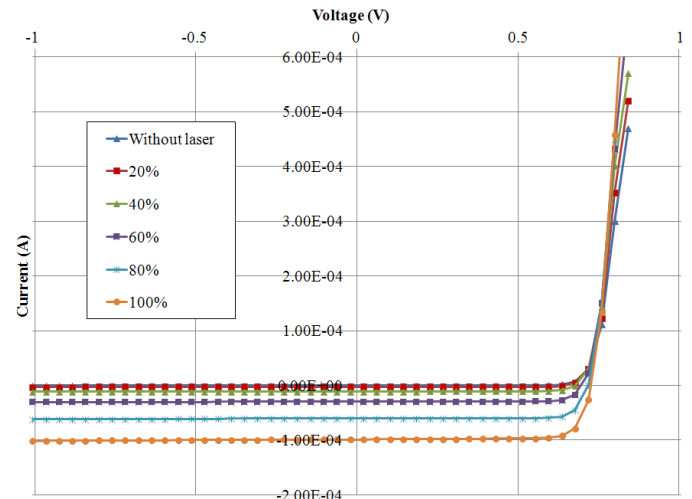

Figure 2: I(V) characteristics of the PN junction under PLS for different laser power.

In order to validate TCAD simulation process flow of the diode under PLS, a structure of a N+ implant on Psubstrate diode extracted from a TCAD simulation process of an NMOS transistor is created thanks Sentaurus Process tool, reproducing all process steps used to build the device.

The aim of this simulation was to reproduce the photocurrent induced in the SCR of the device. In this work, Synopsys simulation tools are used and especially Sentaurus Device Editor (SDE) for grid generation and SDevice for device simulation. The simulated device is a Drain/Psubstrate (or Source/Psubstrate) junction obtained by removing the gate and taking half of an NMOS transistor from a STMicroelectronics 90nm CMOS technology (See fig. 3). Advantages to proceed this way are that a single structure is generated and information about phenomena taking place in the diodes present in an NMOS transistor is obtained.
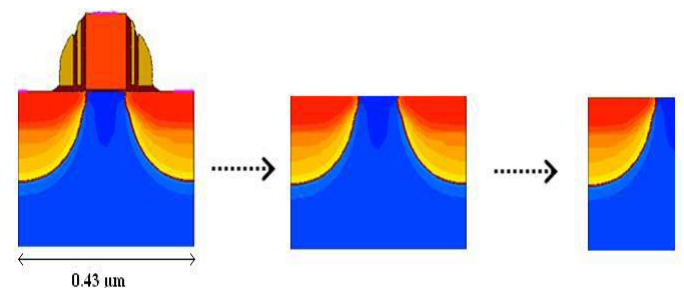

Figure 3: Structure used for diode TCAD simulation.

Current versus voltage characteristics of the diode are simulated in function of the laser power (from $1W.cm^{-2}$ to $30W.cm^{-2}$) of the 1064nm wavelength simulator smooth wave (See fig. 4). Results have the same behaviour than measurements. Therefore this result is a good validation of the TCAD simulation flow developed [5].
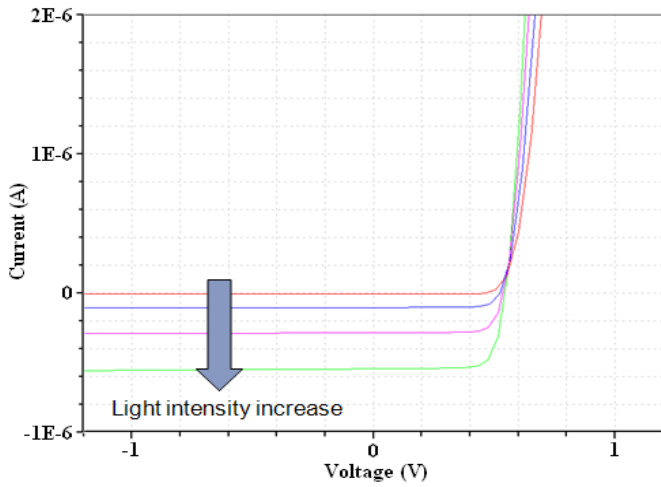
Figure 4: TCAD I(V) characteristics of the diode under PLS for different laser power .

Moreover, in reverse mode, the evolution of the photoelectric current generated in the diode versus the laser power is not linear. From measurements, it is indeed possible to approximate it by a second order polynomial function presented in (1).

$$I_{laser} = 5.10^{-8} * P_{laser}{}^2 + 4.10^{-7} * P_{laser} - 4.10^{-7} \qquad (1)$$

Where I_{laser} is the photoelectric current generated in the PN junction by the laser in Ampere and P_{laser} is the laser power in W/cm².
The same behaviour (second order polynomial behaviour) can be observed thanks TCAD simulation on Drain/Psubstrate photocurrent. The graph on figure 5 depicts the photoelectrical currents obtained from both TCAD simulation and measurements versus the laser power. The values reported on both axis are normalized. It reveals a difference between physical simulation and measurements. This may result from the difference in the target's area exposed to the laser beam: in TCAD simulation the whole junction was exposed to the beam, whereas the beam obtained experimentally has a reduced effect area on the junction.
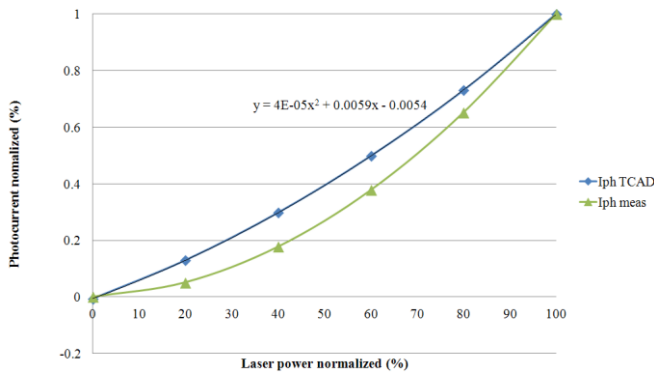

Figure 5: Photocurent generated on a N+/Psubstrate junction extracted from TCAD simulation by comparison with measurements for different laser power.

In first approximation, and only with small laser power on this technology, it is possible to highlight the fact that in reverse mode the diode generates a constant photoelectric current independently of the voltage applied to its two electrodes.

Study of the spatial dependence of the induced photocurrent
The distance between the laser spot and the PN junction has a strong impact on the value of the generated photocurrent. In the following, this effect is studied for N+/Psubstrate junction. When the laser beam is centered on the PN junction (Drain/Psubstrate junction of an NMOS transistor), the photocurrent is maximum, and when the laser moves outside the junction the value of the photocurrent decreases. (fig. 6).
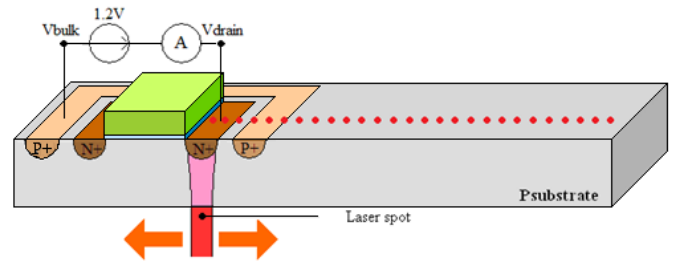

Figure 6: Schematic presentation of the experiment in order to know the spatial effect of the laser on a PN junction.

In order to model the spatial dependence effect on a Drain/Psubstrate diode (N+/Psubstrate junction), an NMOS transistor with long channel (W=L=10μm) was used. The measurements were made with the drain at 1.2V, the Psubstrate bias grounded, and the two other electrodes left floating. The laser spot was moved on a line from the center of the junction to a distance of 300μm. (See Fig. 6). For each step, the photocurrent was measured. This experiment was conducted for the three objectives of our I-phemos laser equipment (2.5X, 20X, and 50X). The obtained photocurrent versus distance curves are depicted on figure 7 after normalization according the maximum photocurrent (Iph2.5X, Iph20X, and Iph50X). Their shapes exhibit a Gaussian-like behaviour.
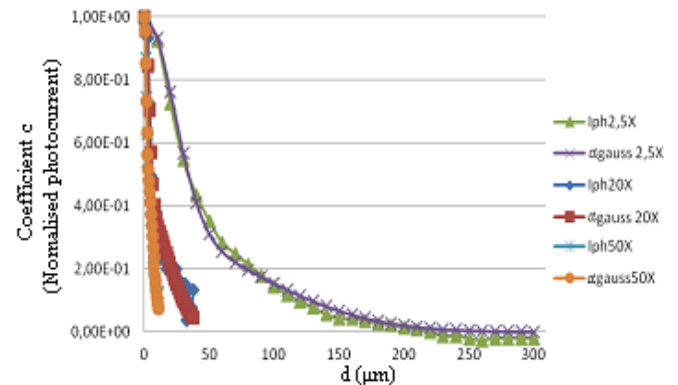

Figure 7: Gaussian effect of laser on silicon according to the I-phemos objective used.

It makes it possible to extract a mathematical model based on the sum of two Gaussian functions (2), where d is the distance between the spot and the closest edge of the junction expressed in micrometer:

$$\alpha_{gauss}(d) = a * \exp\left(-\frac{d^2}{c_1}\right) + b * \exp\left(-\frac{d^2}{c_2}\right) \qquad (2)$$

For each I-phemos objective, the coefficients a, b, c_1 and c_2 were found different (see Table I).

Table I. Coefficients of the Gaussian function (2) for the different I-phemos objectives for the Drain/Psubstrate study.

	2.5X	20X	50X
a	0.4	0.6	0.7
b	0.6	0.4	0.3
c_1	2.5	23.8	1000
c_2	55	654	15000

The Gaussian profile of laser interaction with silicon takes into account the effect of PLS in the area where the diffusion phenomenon occurred (on the both side of the PN junction).
The diffusion length of minority carrier characterizes the distance which could reach photo generated carriers before the recombination process.
In this way a TCAD simulation of a PN junction under a constant backside illumination was performed (See fig. 8). The laser wave was simulated as a plane wave. Due to simulation constraints, the laser area of effect extends over the whole structure. Therefore, the size of the component was changed (and so does the laser beam range) to simulate different spot sizes. The variable of the simulation is the parameter x expressed in micrometer, which define the volume of Psubstrate (in his case, the value x evolved from 0 to 10µm). Then the photocurrent generated on the PN junction is extracted versus the Psubstrate volume. (See fig. 9).
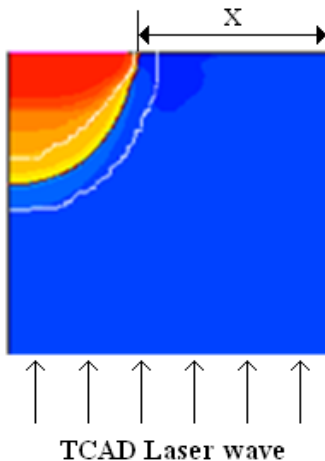

Figure 8: Structure for the TCAD simulation of the photocurrent generated on the PN junction under PLS versus the volume of Psubstrate.

The value of the photocurrent generated on the PN junction increases as x increases from 0 to 1µm. After 1µm, which is approximatively the diffusion length of a PN junction the photocurrent is constant versus the silicon volume.
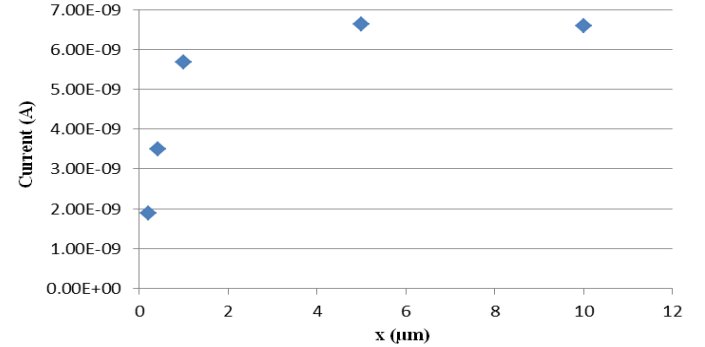

Figure 9: TCAD simulation of the photocurrent generated on the PN junction versus the silicon volume.

The fact that the photocurrent increases only when the value of the distance x (presented on figure 8) is approximatively under the diffusion length of the PN junction, highlights the phenomena of electron-hole pairs collection in the diffusion volume. Therefore this effect participates to the Gaussian behaviour of the photocurrent versus the distance to the PN junction and is not negligible. Its effect on the terms of equation (2), is taken into account by our model, thanks to measurements presented figure 7 [6].

Electrical model of a PN junction under PLS
In order to simulate a PN junction under PLS, the solution proposed in this paper is to define a sub circuit to emulate the source or the drain photocurrent generation. This sub circuit contains a current source whose intensity value is defined for both by the parameter *Iph_val* (3):

$$Iph\_val = S * I_{laser} * \alpha_{gauss} \qquad (3)$$

Where S is the junction area in µm², I_{laser} is the value of the photocurrent generated on the PN junction (as defined in (1)) in Ampère, and α_{gauss} the spatial dependency coefficient (cf. (Equation 2)).
The photocurrent generated on source and drain electrodes takes into account the value of the junction area S and the coefficient c which depends on the distance parameter d chosen by the user for the two junctions of the NMOS, as noticed in equation (2). Coefficient a, b, c_1 and c_2 are defined in Table 1.

Electrical model of an NMOS transistor under PLS

Building the electrical model of the NMOS under PLS
After the calibration step of the sub circuit which model a PN junction under PLS, it is possible to model a 90nm technology NMOS transistor under laser illumination on the basis of

manufacturer technological MOS models. On the four NMOS electrodes, two sub circuits modeling its two N+/Psubstrate junctions under PLS are connected respectively to the source and the drain nodes (Fig. 10).

When the user calls these sub circuits in the main netlist, for each junction (Drain/Psubstrate and Source/Psubstrate) he has to set two parameters: the value S (area of the junction), and d (shortest distance between the centre of the laser spot to the edge of the junction).
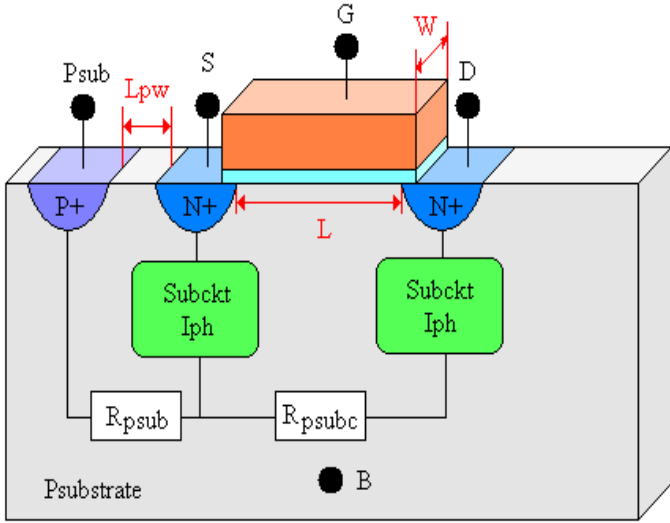

Figure 10: ELDO model of the NMOS transistor under PLS.

Values of the two resistances of the model presented on the figure 10 are defined as following (with geometrical parameters in micrometer defined on figure 10):

$$R_{psubc} = R_{psub}^{\square} * \frac{L}{W} \qquad (4)$$

$$R_{psub} = R_{psub}^{\square} * \frac{L_{psub}}{W} \qquad (5)$$

Where $R_{psub}^{\square}$ is the value of the resistance of the Psubstrate for one square.

Therefore the model takes into account the NMOS size, the location of the laser beam on the device, and its biasing.

Electrical model versus measurements

It is thus possible to simulate electrically the effect of the laser on an NMOS transistor in 90nm technology and to perform a lot of variation on the laser parameters, as the laser power, the beam position, the diameter spot size (via the I-phemos objective chosen). It is also possible to modify the bias condition of the transistor or to change its geometrical dimensions. The aim of this section is to compare electrical simulations with measurements.

The relationship between the photoelectric current induced in the PN junction and the laser power is not linear as equation (1) shows.

In order to show the influence of the laser power on the photocurrent, an NMOS W=10µm/L=0.1µm transistor is used in measures as in electrical simulations. This NMOS transistor is turned OFF. The drain is at the potential of +1.2V, the source, the gate and the bulk (Psubstrate) are grounded.

The photocurrent on the four MOS electrodes is measured according to the laser power, by measurements and by simulations. The objective chosen is the 20X, parked in the middle of the transistor [5].

The graph presented figure 11 shows the very good correlation between electrical simulations and measurements.
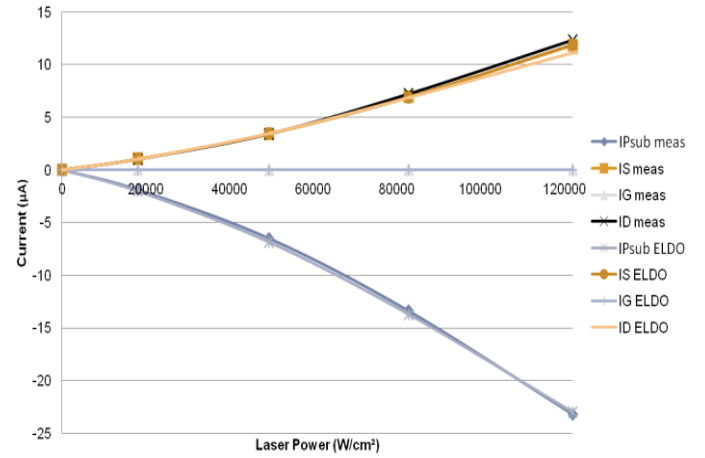

Figure 11: Evolution of the photocurrent for measures in comparison with electrical simulation (ELDO) of an NMOS W=10µm/L=0.1µm transistor polarized OFF versus the laser power.

Both photocurrents measured at the transistor's drain and source were found equal. It reveals that the laser spot was at equal distance from both drain and source. Moreover, the current conservation law (eq. 6) is fulfilled at any laser power [7, 8].

$$|I_{substrate}| = I_{drain} + I_{source}. \qquad (6)$$

Measurements of the photocurrents for different NMOS transistor gate lengths with the same area of N+/Psubstrate junction, were performed with identical biasing. The NMOS was turned off (drain at +1.2V and the three other electrodes grounded). The laser was set at its maximal power, and parked in the centre of every transistor.

Because of the Space Charge Region (SCR) located under the gate, the area between source and drain has an impact on the photocurrent generated by the junctions. Indeed, the photocurrent was found stronger for transistors with bigger gate areas as shown in figure 12.

An hypothesis is that a part of the total amount photocurrent collected from source and drain electrode is coming from the channel depletion region [5].
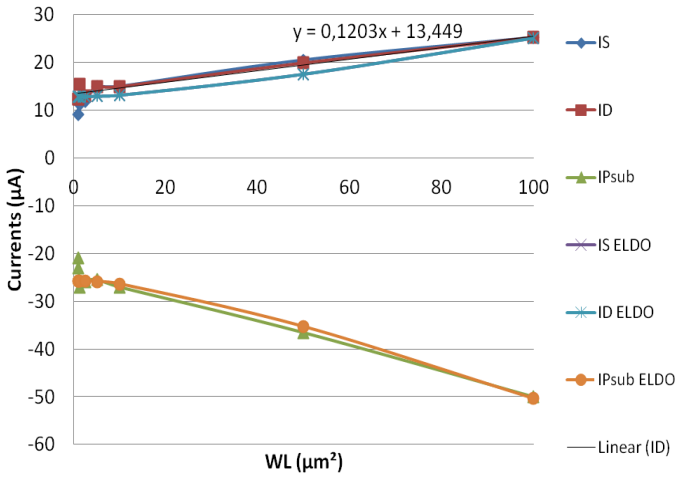
Figure 12: Comparison of the photocurrent evolution according to transistor lentgh between electrical simulations (ELDO) and measurments.

It is possible to extract a linear estimation of this curve which is given in (7).

$$y = 0.1203 * x + 13.449 \tag{7}$$

So an additive term expressed in (7) is added to (3) in order to obtain equation (8):

$$Iph\_val = (S * I_{laser} + Iph\_gate) * \alpha_{gauss} \tag{8}$$

Iph_gate is a linear function proportional to the area under the gate. (8), obtained from (7).

$$Iph\_gate = 0.1203 * W * L \tag{9}$$

Figure 12 also shows that the effect of the area under the gate is well modelled by the electrical model.

Current cartographies

The aim of drawing 3D electrical current cartographies is to predict the correct behaviour of a device under test simulation independently of its location. It may serve as a "golden" reference to detect any defect by comparison and measurements.

Principe of electrical 3D current cartographies
The principe of the electrical model of cartography lies in the creation of a mesh on the layout of the transistor. The step of the meshing is a parameter called *stepXY* defines in the ELDO netlist. It is necessary to calculate in every point of the mesh two values of distance. The shortest distance between the centre of the laser spot and the edge of the drain junction, and the source junction.

To illustrate the principe of cartography, it is possible to take an example on an NMOS W=10µm/L=10µm transistor. Three cases are envisaged. The first one, is when the laser spot is parked on the centre of the drain junction. The second, when the laser is positioned on the source, and the last one when the beam is centred in the middle of the NMOS transistor. For each case, drain, source and Psubstrate currents were extracted from the ELDO simulation (See Fig. 13) [9].
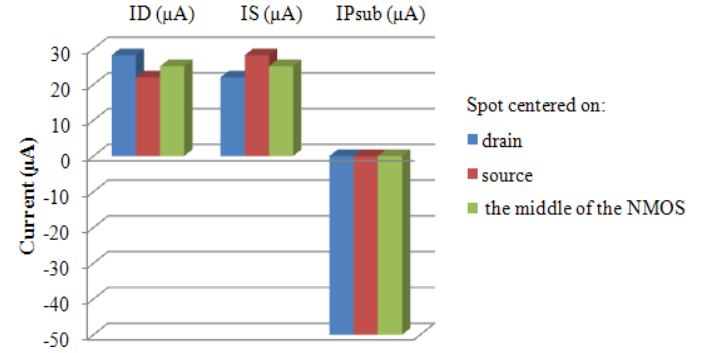

Figure 13: Electrical simulation thanks to ELDO for different localisation of the laser spot.

In a simple case as this one where the meshing is established by only three aligned points, it is possible to define the parameters d_d (distance of the centre of the laser spot to the closest edge of the drain) and d_s (distance of the centre of the laser spot to the closest edge of the source).

$$d_d = m.stepXY \tag{10}$$

$$d_s = L - m.stepXY \tag{11}$$

In this case *stepXY* is equal to 5µm, with *m* being a parameter evolving between 0 and 2 by step of 1. *L* is the gate length of the NMOS transistor expressed in micrometer.
When the laser beam is centered in the middle of the drain, the photocurrent generated by the drain is more important than that the source, and the preservation of currents is respected (6). If the beam is centered on the source junction, it is the photocurrent generated by the source that is more important than that generated by the drain, always by respecting the preservation of the currents (5). In the last case, when the laser beam is centered in the middle of the NMOS, the photocurrents generated by the source and the drain are identical (12).

$$I_{PSUB} = 2 * I_S = 2 * I_D \tag{12}$$

On the same principe, it is possible to create more complex cartographies, by creating a denser mesh. The same method is always used. In every point of the mesh, two values of distances are associated. The first value is the distance between the center of the laser spot to the closest edge of the drain. And the second value is the distance between the center of the laser spot to the closest edge of the source.

3D current cartographies on an NMOS transistor turned OFF

In this section, it is proposed to draw 3D current cartographies (extracted from the ELDO simulator) of photocurrents generated on an NMOS transistor W=L=10μm [8]. It is also possible to extract 3D cartographies of photocurrents generated by the two PN junctions of an NMOS [9].
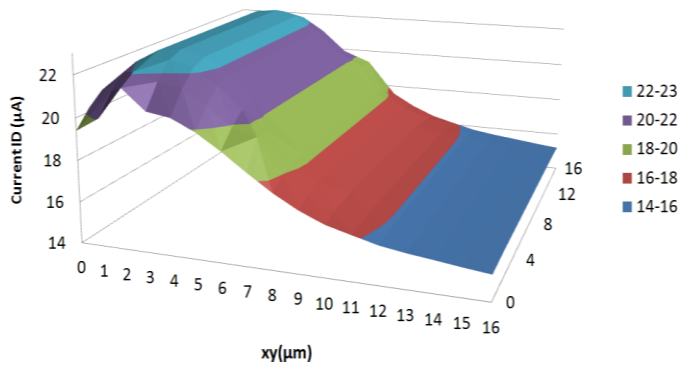

Figure 14: 3D Cartography of the photoelectrical contribution of the source under PLS extracted from electrical simulation (ELDO).
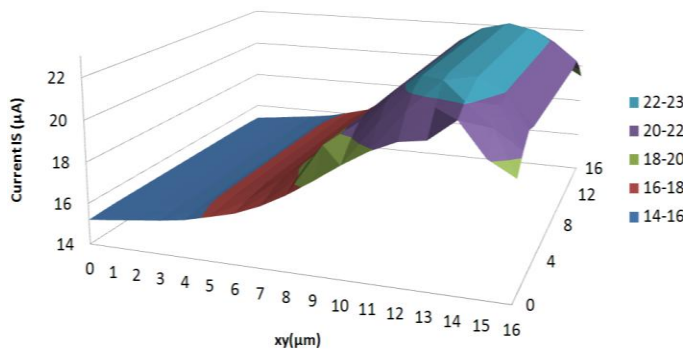

Figure 15: 3D Cartography of the photoelectrical contribution of the drain under PLS extracted from ELDO.

The 3D cartographies of the photocurrent generated in the two N+/Psubstrate junctions highlight the Gaussian shape of the laser amplitude versus the spot location (See fig. 14 and 15).
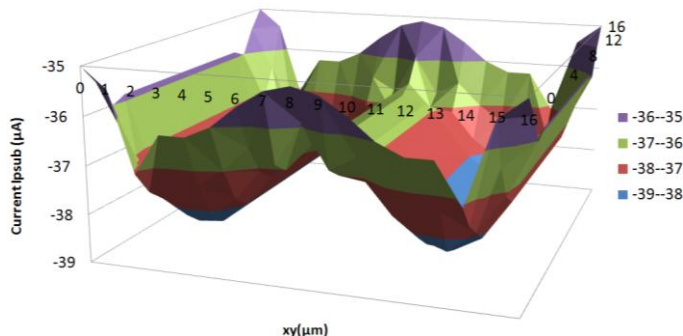

Figure 16: 3D Cartography of the photoelectrical contribution of the Psubstrate under PLS extracted from ELDO.

Conclusion and perspective

The process of building an accurate electrical model of an NMOS transistor in 90nm technology under photoelectrical laser stimulation was reported in this paper. The validity of the approach was assessed by the very good correlation obtained between electrical simulations (based on SPICE language) and measurements. TCAD physical simulations were also ran to explore the underlying physical phenomena. In failure analysis it could have a great utility in order to compare the simulated response of a golden circuit under PLS with actual measurements. This work has been extended to PMOS transistors [10, 11]. Therefore, as a perspective, it will permit us to simulate the behavior under PLS of complex logic gates made of PMOS and NMOS transistors.

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