Robustness of CMOS Circuits Designed for Space and Terrestrial Environment

Jean-Max Dutertre, Fernand-Michel Roche

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J.M. Dutertre, F.M. Roche
LIRMM, Université Montpellier II, 161 rue Ada, 34392 Montpellier cedex 05, France
dutertre@lirmm.fr, roche@lirmm.fr

Abstract

The behaviour of Integrated Circuits (IC), in Space, the high atmosphere or even in earth environment, are adversely affected by radiation. One of the most concerning effect is stochastic, caused by heavy ions of high energy which cannot be shielded. Striking the circuits, the invasive particles induce transient current upsets, being the cause of unpredictable soft errors in combinatorial logic and memory cells. After a brief survey of the phenomenon and its consequences, we report a strategy to improve the hardening capabilities of a standard commercial technology only using a design methodology. We present a new inverter architecture for which robustness is naturally attained during upset. The hardening is carried out through the use of an integrated information redundancy and a double tri-state output. The design prevents errors to propagate and gives an uncorrupted information source. Post layout SPICE simulations of the cells confirm the efficiency of our integrated approach to avoid the induced effect of a pulse shape current generation inside the IC.

1. Introduction

The robustness of Integrated Circuits dedicated to Space has been the object of a considerable amount of attention since the first unexplained failure of satellite due to solar eruptions and unpredictable cosmic rays [1-3]. At this point the problems seemed confined to the space and high atmosphere. Nevertheless, since the works of IBM reporting soft fails in terrestrial computer electronics [4-5], the question became a real priority problem for the circuits dedicated to secure systems or to insure watching functions. Optimising reliability is a challenge for example in aeronautics or medical applications. This question is getting an increasing weight with the regular reductions of scale, voltage and power in the new technologies. The situation is still magnified by economical reasons: the founders being unable to maintain in production an old but verified rad-hardened technology for few components. With systems for which the functional outcome is essential, a redundancy at the system level is generally considered. This increases -more than three times - silicon area, cost and energy consumption of the systems, while the trends are precisely to reduce it with systems on chip.

We propose to use a methodology integrating the hardening and redundancy properties at the design level, taking into account the degradation phenomenon. We present a new inverter architecture compatible with the highly submicronic technology and its superimposed metal layers.

In the following we introduce the different phenomena and focus the study on an effect due to external particles impinging the device. We analyse the degradation of the signal and propose a new inverter cell designed to prevent error propagation.

2. Phenomenon and the sensitive areas

Different radiation effects can take place in ICs. The Total Ionizing Dose effects (TID) due to charge in oxides which can cause threshold voltage shift and current leakage. The Single Event Effects (SEE) induced by a single particle hit in a sensitive area, effects not determinist : among these effects, the Single Event Latch-Up (SEL) and the Single Event Upset (SEU). The SEL is a destructive effect through parasitic thyristor activation while the SEU results in transient current pulse upset on sensitive nodes. Presently, we shall not address TID or SEL corrected by adequate process techniques but the SEU effect which represents a radiation-induced hazard difficult to avoid. Afterwards we shall provide some brief background in the area of SEU mechanisms and describe their implications. Some more details will be found in [6-8].

Three basic concepts explain SEU: energy loss, charge collection and transient upset. When an energetic ion passes through any material it loses energy through interaction with the semiconductor bound electrons. It creates a dense track of hole-electron pairs, which may recombine with no effect. But in the presence of electric fields, typically in reverse biased P-N junction, electrons and holes are drifted in opposite directions and collected at device junctions. The consequence is a transient current pulse. Such an upset drives the drain voltage of PMOS or NMOS respectively to the high or low level. Considering an inverter, the sensitive area is

the drain of the OFF transistor, related to the logic state of the input, as shown in Fig. 1.

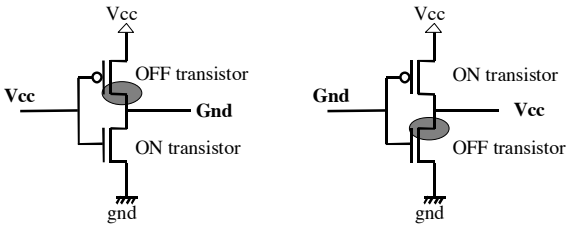

Fig. 1 Location of the inverter SEU sensitive areas.

The resulting voltage transient determines a logic upset being indistinguishable from common signal. So, the logic upset can propagate through for example combinatorial logic, clock or control lines and causes bit flip soft errors.

Because of the random nature of the particle, the effect observed is unpredictable and can not be "tested". So, the hardening must be anticipated on a worst case basis. Fortunately we have to take into consideration the low frequency of the upset, due to the very low value of the particle flux. We shall assume that just one upset can happen at the same time and in the same sensitive area, excluding the case of multiple upsets. The post lay-out SPICE simulation will be conducted using a pulse current source to emulate the SEU at the sensitive node. The simulation can reproduce a charge equal from two to three times the worst event generally observed. The current pulse is fixed at a 10 mA amplitude, 50 ps rise and fall times and a programmable duration.

3. Inverters chain simulation

In this section, we present the post layout SEU simulations of an inverters chain (Fig. 2). Parasitic capacitance extraction was conducted after the circuit was designed using ST Microelectronics 0.25 μm CMOS process. The broken arrow indicates the location of the upset.

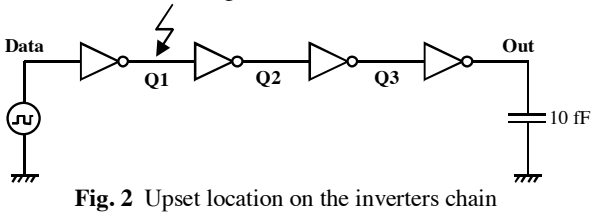

Fig. 2 Upset location on the inverters chain

The results are illustrated on the Fig 3. As expected the standard inverters are very sensitive to upsets. As soon as the perturbation is exceeding a 100 ps duration, which is common, any upset at node Q1 will be propagated up to the output at the extremity of the chain. The current I_{alea} injected on node Q1 to emulate upset results in driving this node to low level during the whole upset duration. The transient voltage is propagating through the three inverters to the output node (see Fig. 3). Mavis et al [9] have shown that even with a larger number of inverters the perturbation will propagate unattenuated. Similar result occurs for upset to high level.

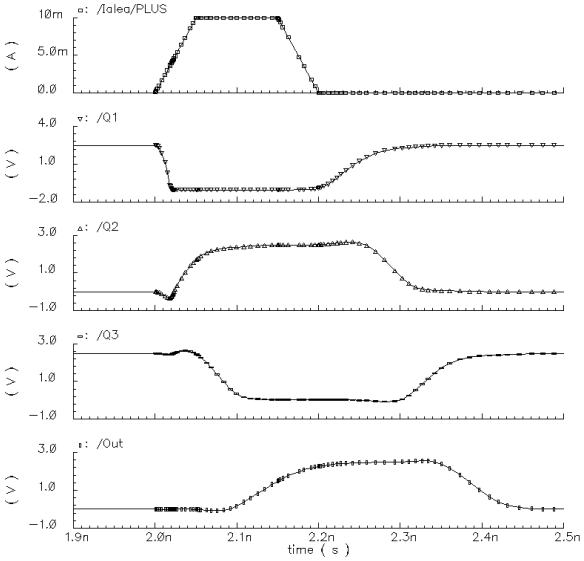

Fig. 3 Upset propagation through inverters chain.

When used into ICs general Clock and Data lines, such inverters need to have the integrity of their signal preserved across the whole circuit. Thus upset propagation along inverters chains is a main issue when hardening . In the next section, a SEU hardened design to cope with this outcome will be detailed.

4. The SEU hardened HZ inverter

A. Description

Some hardened CMOS inverters have been presented in the past few years [10-15]. We propose here a new design which on a simulation basis can be advantageously compared with the previous issues. Hereafter, the hardening is completed through the use of two techniques: an information redundancy and a tristate double-output, respectively for protecting the information and preventing an error propagation. (Fig. 4).

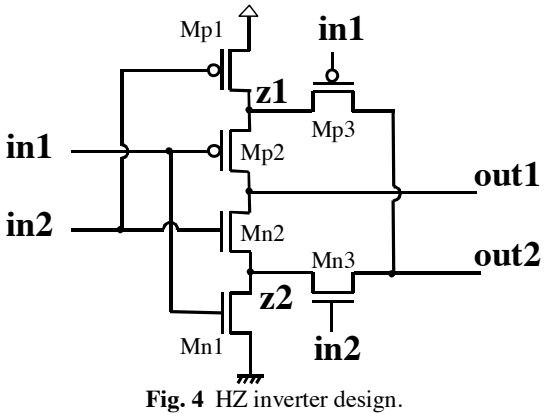

Fig. 4 HZ inverter design.

If the two inputs have the same logic level, the circuit works like an inverter, with the two outputs established in the complementary logic state. The truth table (Table 1) makes this point obvious, and the fact that as soon as the inputs have not the same status, the outputs are switched onto a high impedance state. So, if a single transient arises from anyone of the inputs, it acts turning the HZ inverter outputs in the high impedance status, preserving the logic state and stopping upset propagation. This design has been named HZ-Inverter with reference to this high impedance status.

In 1	In 2	Out 1	Out 2
0	0	1	1
0	1	HZ	HZ
1	0	HZ	HZ
1	1	0	0

Table 1. Truth table

Alike the standard inverter, the HZ-Inverter has its SEUs sensitive areas located on the OFF-transistor drains (Fig. 5).

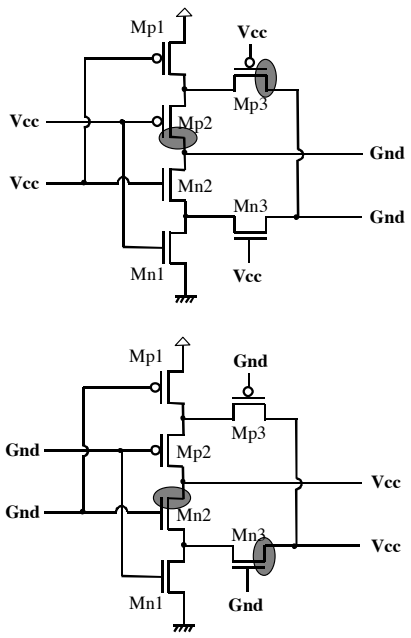

Fig. 5 HZ-Inverter sensitive area according nodes voltage

SEU may arise on only one sensitive node at the same time (out1 or out2), however its propagation will be impossible in a chain of HZ inverters as the following simulations show.

B. Simulation of an HZ inverters chain

A layout of HZ-Inverters is completed with the same CMOS process. The parasitic capacitance is extracted and SPICE simulations run to verify functionality and hardening capabilities. For comparison purpose, a chain of four inverters is used (Fig. 6). The broken arrow indicates the nodes (Q1 and Q11) where the upsets are simulated. Various pulse durations are applied.

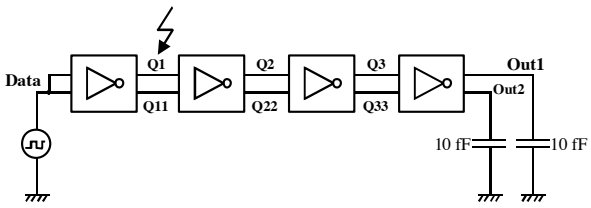

Fig. 6 HZ inverters chain and upset location.

The Figure 7 illustrates the effect of an upset on node Q1 for a 2000 ps pulse. Upset drives the Q1 node voltage to low level, while node Q11 undergoes only a negligible voltage perturbation; its state remains high. Nodes Q22, Q33 and Out2 voltages were not drawn as they are respectively the same than the nodes Q2, Q3 and Out1 voltages. The little increase of Q2 (and Q22) voltage is not sufficient to flip the third inverter of the chain.

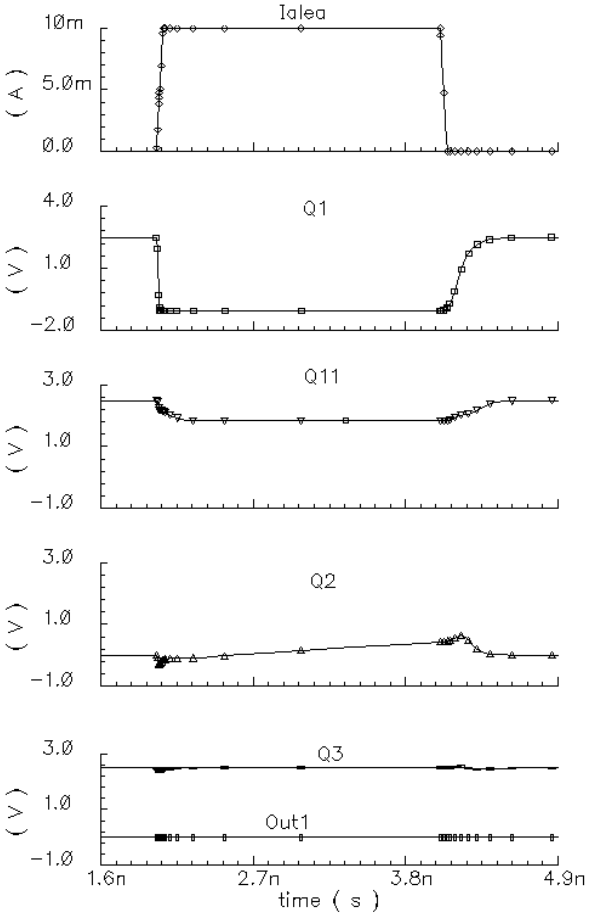

Fig. 7 Simulation of a 2000 ps upset on node Q1

These simulations show that even an upset of 2000 ps duration and 10 mA amplitude on node Q1 will not propagate. This duration is far beyond the specifications of a realistic SEU.
All the upsets susceptible to exist on nodes Q1 and Q11 from 1 to 0 and 0 to 1 have been simulated and they do not propagate until a 3500 ps duration, which is out of the realistic conditions.
This proves the efficient robustness of the HZ inverter. When used in global clock or data lines it will prevent the upset propagation across the whole circuit, as we shall see now.

C. Performance of the HZ inverters chain

So consider the previous HZ-Inverter set as a Clock-line with a 200 MHz signal frequency and submitted to successive upsets during the static and dynamic regimes. The Figure 8 illustrates the better and the worst cases: A 500 ps pulse during the static regime and a 500 ps pulse during the rising edge transition. The first perturbation is completely absorbed preserving the integrity of the Clock. The second perturbation induces just a delay in the signal transmission. In the both cases, no untimely effect is observed while Standard circuit will exhibit glitches in the same conditions. So if care is taken in design to set-up and hold times, no adverse effect on the IC functionality will be efficient

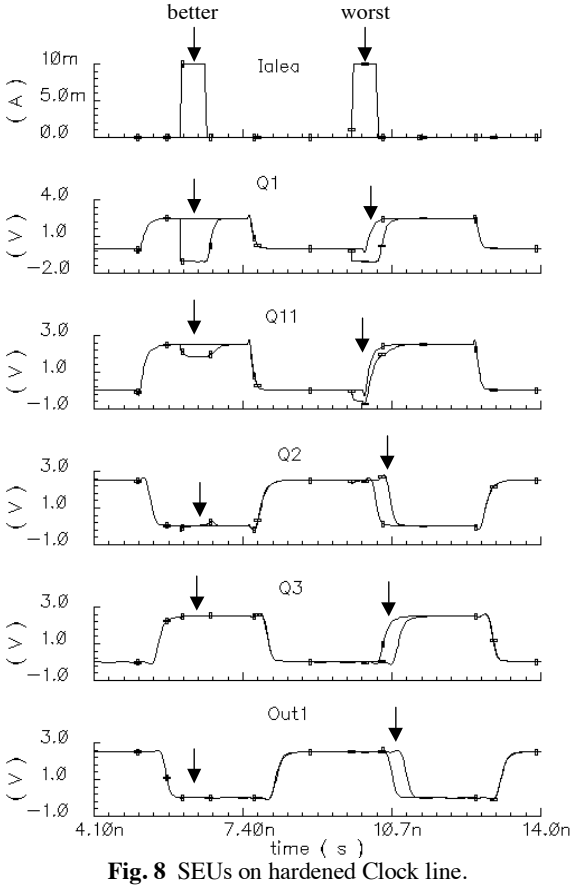

Fig. 8 SEUs on hardened Clock line.

The major drawback of the HZ inverter is its area compare to standard inverter area. The Figure 8 gives the layouts respectively of the standard inverter and the HZ inverter for comparison purpose.

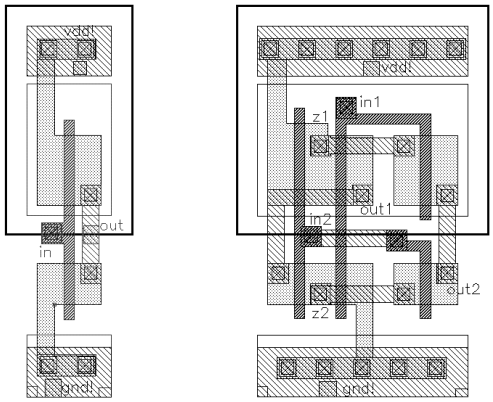

Fig. 9 Layout of the classic and HZ inverters.

Another object of concern is the cell area. The HZ inverter area is 45 μm^2, about twice and half the standard inverter area which is 18 μm^2.But the area must be compared to a corresponding redundant circuit including three Standard inverters and the voter, wich consumes a large area. Excluding the hardening of the voter the area of the standard redundant circuit can be estimated to more than the double of the HZ inverters equivalent.

5. CONCLUSION.

In this paper we have presented the use of design techniques to solve the SEU hardening problem. They only apply to design at circuit level, therefore no fabrication process development is required. The HZ-Inverter proposed exhibits a very efficient hardness to SEU propagation, as SPICE simulations show. One major interest of this cell is its ability to be easily integrated in design where a dual and sequential transfer of the level is not a challenge. It will be worthy in IC for which absolute hardness assurance against upset is required.

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