Improving an SEU Hard Design using a Pulsed Laser

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Abstract-- **The purpose of this work is to present one investigation utilizing a pulsed laser as a tool to improve the Single Event Upset tolerance of a memory cell. These results coming with a previous ion testing evaluation of the circuit allow an optimization of the design. The laser results permit a more detailed analysis of the phenomenon leading to the upset and a precise localization of the most sensitive areas. As a result the behavior verification of the design combined with the use of robust elementary blocks strengthens the hardening capabilities of the cell.**

I. INTRODUCTION

In the past a considerable amount of efforts has been directed towards the improvement of the SEU rad tolerance of SRAMs [1-8] or basic devices for combinational logic [9]. The topic is still of interest due to a size scaling of the commercial technology. Furthermore the pulsed laser tool has become mature to collect information about the Single Event Upset (SEU) behavior of a wide range of integrated circuits [10]. The advantages of this technique have been exhaustively studied and detailed in particular by Melinger, Buchner, McMorrow of NRL and other teams [11-15]. With the object of improving the circuit hardness assurance, one of the main benefit of the laser use is the ability to locate the sensitive area - and consequently the electric node involved - in a *deterministic* way compared to the random nature of upsets induced by ions during synchrotron experiments. As a consequence, this tool of investigation brings convenience, consistence and repeatability .

In this paper we report on a set of experiments performed at the IXL Laboratory using laser facilities to determine the threshold sensitivity of chips previously evaluated in particles accelerator. The circuits presented hereafter have a flip-flop configuration and are fabricated in a *commercial unhardened* CMOS 0.7 μm technology. The tests described in this paper

are part of a library design optimization (on this subject the reader could refer to the chart of McMorrow et al. [14]). The laser is used to draw up a map revealing the threshold location. Then the upset mechanisms and the sensitive nodes are identified making possible an adjustment of the design parameters for improving hardness assurance.

II. METHOD

A. Device Description

The test vehicle consists of twelve independent shift registers. Each of them combine a set of 40 D-latches organized into 20 flip-flops [16]. Half of the registers are designed with CMOS standard cell D-latches (Fig.1), the other half with rad tolerant ones (Fig.2).
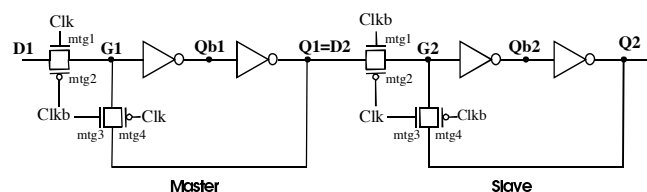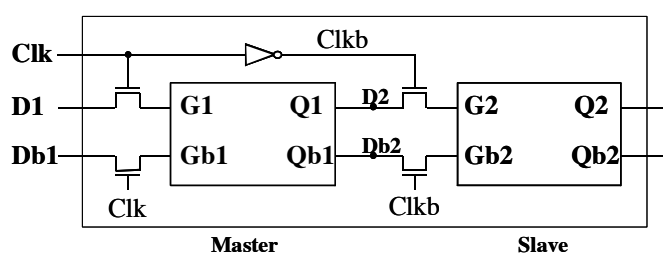

Fig. 1. Standard flip-flop.

Fig. 2. Hardened flip-flop featuring the two rad hard latches.

The two latches form the memory cells of the flip-flop. An examination of these cells at transistor level allows us to locate the specific design areas that are SEU sensitive when exposed to the hit of an energetic particle. These areas match the reverse biased junctions of both the access transistors and the memory latches. Their locations change according to the logic state of the nodes. Summarizing, PMOS junctions at low level are liable to be driven to high voltage when hit by energetic ions (respectively NMOS junctions at high level are

liable to be driven to low voltage). The sensitive areas or nodes are pointed out on figures 3 and 4 according to the electrical state of the nodes.
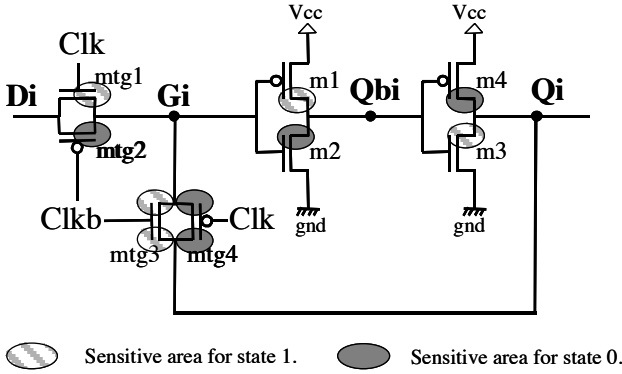

Fig. 3. Standard latch design and location of sensitive areas.

In the following, to give a simple description of the logic "status" of the nodes a standard D-Latch will be said in the state 1 if Qi=Gi=1 with Qbi=0, and in the state 0 when Qi=Gi=0 with Qbi=1. In a similar way a rad hardened latch will be said in the states 1 and 0 respectively if Qi=Gi=1 with Qbi=Gbi=0, and if Qi=Gi=0 with Qbi=Gbi=1.
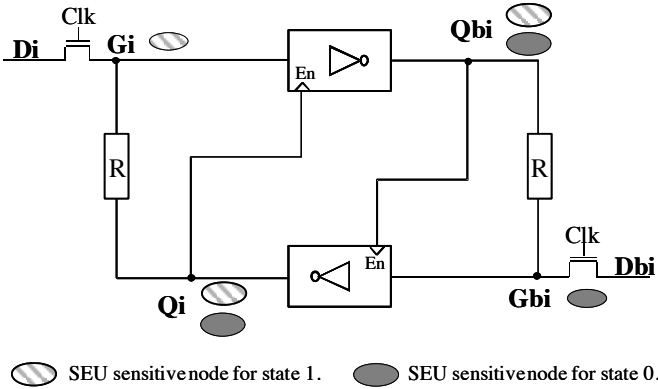

Fig. 4. Rad hard latch design and sensitive nodes.

To achieve SEU hardness this last cell combines two distinct techniques : a RC filtering and a switching into a high impedance state. The RC filtering prevents the feedback loop from causing a bit flip in case of an upset on nodes Qi and Qbi. The circuit-switching into a high impedance state also prevents any transient bit flip from stabilizing. As a matter of fact, when the node Gi (Gbi) storing a 1 is upset to 0, Qbi (Qi) is brought into a high impedance state ; so, its logic state is kept safe during the disturbance, then the Gi (Gbi) node value is restored. Ground test were performed at the Lawrence Berkeley Laboratory 88'Cyclotron [16]. The experimental results show that this design approach was relevant to achieve SEU hardening capability, as the SEU Linear Energy Transfer (LET) threshold of the hardened flip-flop was up to 27 MeV.cm^2/mg while the standard flip-flop presents a LET threshold of 6 MeV.cm^2/mg.

B. Experimental conditions

The laser test is carried out using a Ti : Sapphire pulsed laser delivering 1ps width pulses with a central wavelength of 800 nm. The penetration depth is estimated to 12 μm. The beam is focused by a 100X microscope lens objective down to 1μm above the surface of the device under test. A CCD camera coupled with the microscope objective allows us to visualize the impact point. The scanning resolution is 0.2μm. The upset detection is carried out by checking the electric state of the register output on a Slave. For each strike location producing an upset the corresponding point is colored on a map. The red points corresponds to the sensitive points, i.e. the lower energy sensitivity areas.

The laser test is performed with a clock set down in state 0 corresponding to the static mode of the memory cell. The Master latch is settled in a well established memory mode while the Slave latch is in a write mode. So, the value memorized by the Master is permanently written in the Slave. This usual pattern has an impact on the experimental results expected.

On the one hand, if an upset arises at the Master level, the wrong value will be stored and the erroneous value transferred to the Slave ; and, for laser testing the error will be rightfully identified as coming from the Master.

On the other hand, a bit flip of the Slave state will not be traceable if the correct value is still stored in the Master because of a permanent writing of the Slave to the right value before an error transference to the output. One must be prepared to see the observed laser sensitive areas confined in the Master part of the map.

III. EXPERIMENTAL RESULTS

Some maps of the *standard flip-flop* sensitive areas are presented on Figure 5 with a microphotograph of the layout. The result evidences the sensitivity evolution of the Master nodes of the figures 1 and 3, for energies starting from 9 pJ up to 50 pJ. The picture draws the outline contour of contacts, via and metal interconnects of the cell, as laser is reflected by metallization. But the map of Figure 5 exhibits also unexpected sensitive regions of the Slave - areas D2 and G2 (state 1). In principle these upset areas should not be observable. Indeed, the sensitivity mapping being conducted in static mode, any flip of the Slave should be corrected by the Master. The observation of points on the map in the Slave area means that the Master itself was flipped too. In turn the Master is imposing its new false state onto the slave. Then the upset is detected and the point is colored on the map as coming from the Slave.

This indirect phenomenon, made clear for the first time, is due to a "back-generation" of the transient effect by the *circuit structure*. This interpretation will be confirmed by the SPICE simulations of the section IV (see Fig.7).
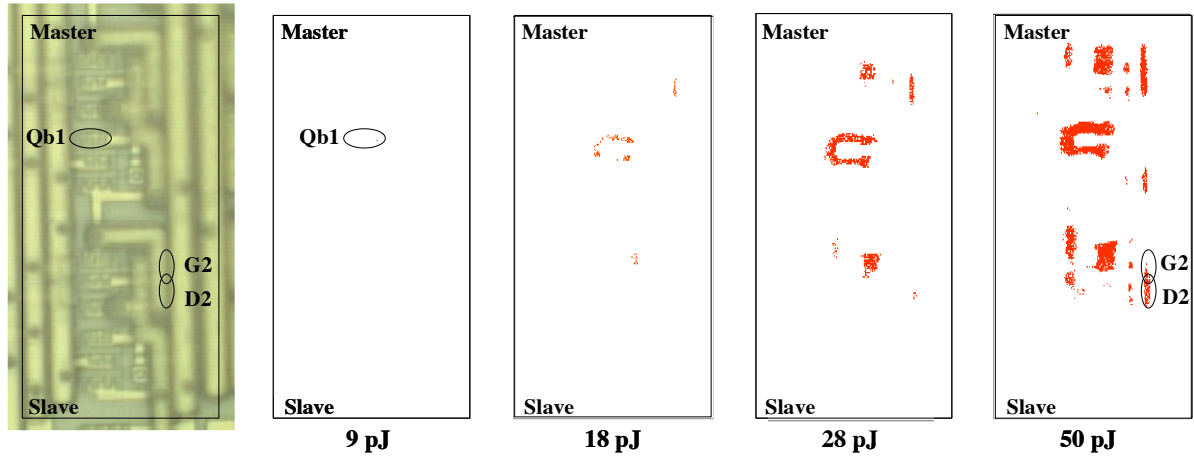
Fig. 5. Standard flip-flop layout and SEU sensitivity mapping of the state 1 at different energies.

In a parallel experience, a laser mapping of the *hardened flip-flop* (Fig. 6) still makes manifest the presence of some sensitive zones on the Slave (G2 and D2 in the state 1, with Gb2 and Db2 in the state 0) bringing to the fore the existence of the same phenomenon of back-generation from the Slave to the Master despite the hardened design of the cells.

Moreover one may also observe the existence of similar sensitive areas on the nodes Q1 if the Master is in the state 1 and on the node Qb1 if in the state 0.

Table 1 lists the different areas which are SEU sensitive, and the observed energy thresholds for states 1 and 0. An increase of the laser pulse energy beyond 50 pJ does not reveal other sensitive area; the only effect to mention is an extent of the former ones. If we apart the G1 area because of its high occurence value (50 pJ) , the SEUs concern mainly the Q1 area in state 1 and the Qb1 area in state 0. Following our previous remark regarding back-generation this observation becomes noticeable on hardened circuit since areas D2 and G2 are connected to Q1 and respectively areas Db2 and Gb2 to Qb1 (Fig. 2 and 4).

The experimental results are confirmed by the SPICE simulations of the section IV (Fig. 8 and 9).

TABLE I

SEU SENSITIVE AREAS OF THE HARDENED FLIP-FLOP AND THEIR CORRESPONDING ENERGY OBSERVATION THRESHOLDS

State 1		State 0	
D2	17 pJ	Qb1	27 pJ
Q1	30 pJ	Db2	30 pJ
G2	30 pJ	Gb2	30 pJ
G1	50 pJ		

IV. ANALYSIS AND SIMULATIONS

When we analyze more tightly the behavior of the *standard flip-flop* under laser exposure, the presence of a SEU sensitivity is observed on D2 but also on G2 of the Slave. Indeed the electrical disturbance propagates from G2 through the transmission transistors mtg1 and mtg2 to D2 and Q1 (see Fig.1) and finds propitious conditions for a permanent switching of the Master. This interpretation has been confirmed by SPICE simulations of an upset on the node G2 with a flip-flop in the memory mode (Clk=0, Clkb=1) storing the logic state 1. The sensitivity is effective for a (600ps, 2mA) current pulse applied between node G2 and the bulk (gnd).
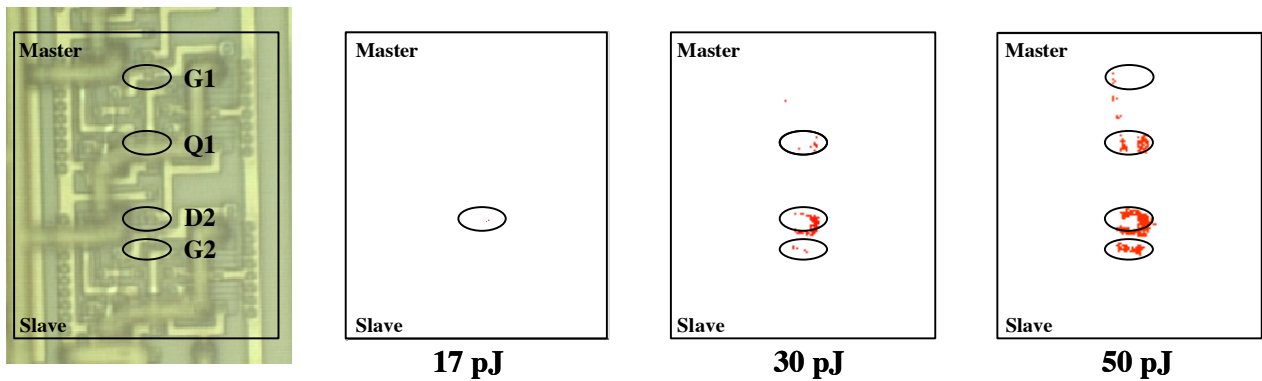

Fig. 6. Hardened flip-flop layout and SEU sensitivity mapping of state 1 at 30 pJ, 50 pJ and 70 pJ.

The simulation data of the *standard flip-flop* presented on figure 7 show that the rapid decrease of G2 to 0V pulls down Q1, inducing a switch of the Master latch. So, an upset on the Slave involves a definite change of the bit memorized by the Master.
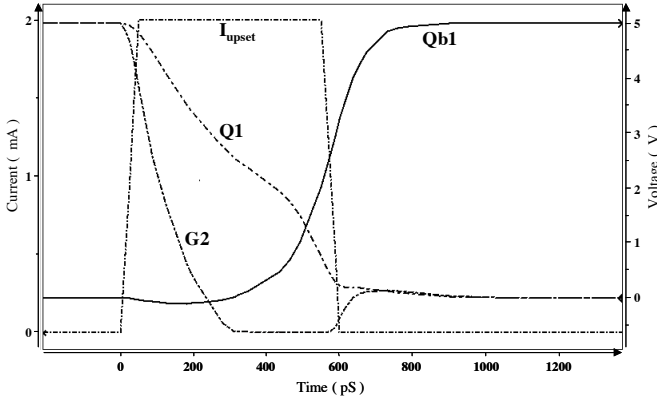

Fig. 7. Upset 600 ps 2 mA on node G2, standard flip-flop, state 1.

Now, if we look at the laser results of the *Hardened flip-flop*, in state 1, we observe that in the flip-flop configuration the more appealed node is the node Q1 of the *Master latch*. Many laser impact areas are related to this node and its electric state while in state 1 (respectively Qb1 in state 0).

The figure 8 illustrates in detail the permanent flip of the Master. The rapid decrease to 0V of Q1 voltage pulls down G1 voltage, inducing a permanent change of the Master latch. As a matter of fact the upset on node Q1 is propagated to node G1 despite the RC filtering, due to a persistence of the upset (600 ps).
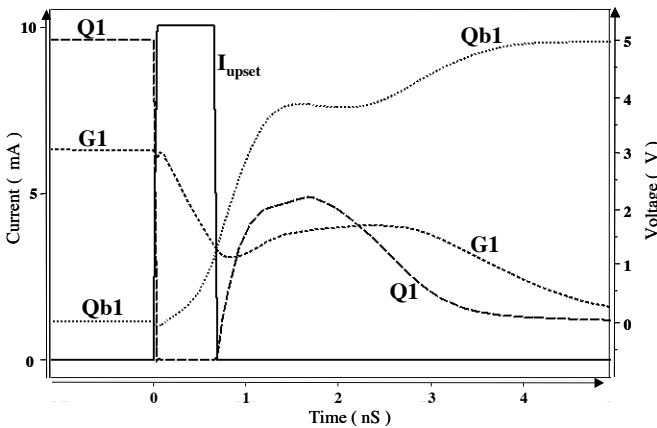

Fig. 8. Upset 600 ps 10 mA on node Q1, hardened flip-flop, state 1.

Note that in a previous paper [16], the hardening assessment of the *basic hardened latch* of this flip-flop was successfully simulated and found "immune" through post layout SPICE simulations, while the very same hardened designs organized in a register of flip-flops were tested SEU sensitive to a heavy ion irradiation (beyond a LET Threshold of 27 MeV.cm2/mg). This can be explained by the time duration limitation of the pulses fixed to (500ps, 10mA) and even (500ps, 20mA) for simulations.

In the present study the (600ps, 10 mA) current pulse SPICE simulations is in accordance with the 1ps width laser pulse to highlight a SEU sensitivity of the whole flip-flop structure. The above study points out another observation: the evaluation of a circuit sensitivity cannot be done using the sole charge deposited criterion expressed in pC. The boundary conditions must be considered too (see also the approach of Baze and al. [9]).

In a similar way for this hardened structure, we observe that a sufficiently long pulse duration (900ps, 10mA) on the node G2 of the Slave, can also provoke a permanent switch of the flip-flop. This is illustrated on Figure 9. In this circuit, G2 is once again connected to the node Q1 via a pass transistor as it can be seen on figure 2. So, while attenuated a "back-generation" of the upset can still exploit the SEU sensitivity of the node Q1 in state 1 (respectively Qb1 in state 0).
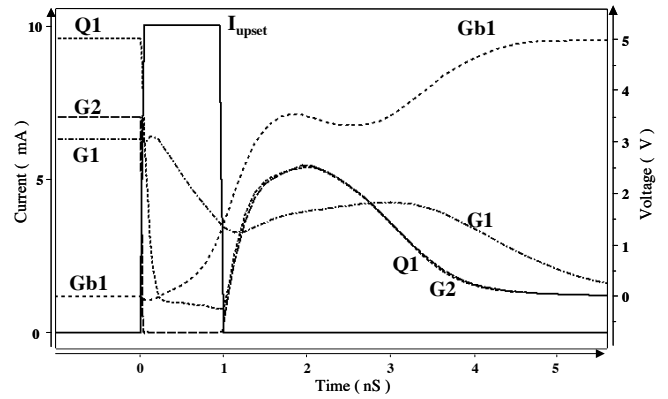

Fig. 9. Upset 900 ps 10mA on node G2, hardened flip-flop, state 1.

In this experiment, the test laser analysis allows first to evidence a SEU back propagation phenomena from the Slave to the Master in flip-flops and then to point out the relative weakness of a RC-filtering in our hardened circuit. All these results permit us to undertake an amelioration of the SEU tolerance as the next section will now present.

V. SEU IMMUNITY IMPROVEMENT

Once the soft error origin is identified and analyzed on laser mapping, we look for the optimal hardening conditions with SPICE circuit simulations taking into account the layout parasitic capacitances. In the present case the sensitivity being caused by a weakness of the feedback circuit, we conclude that an unsuited RC filtering towards the node G1 is the cause of the SEU sensitivity when an upset to zero occurs on Q1 (or from Gb1 to state 0 when an upset to 0 is happening in Qb1). Then the filtering margins are adjusted through a cell resizing using SPICE. New simulations undertaken after intervention on the design are presented on

figures 10 and 11. Checking the immunity on node Q1 of the Master in a new worst case condition of upset will confirm the validity of the diagnosis and the efficiency of the hardening solution.
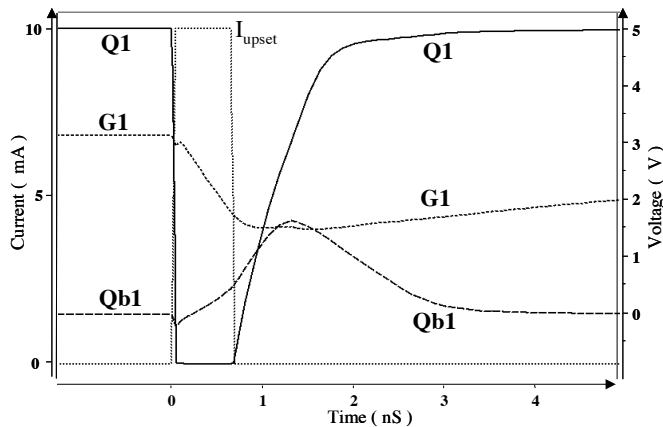

Fig. 10.   Upset 600ps 10 mA on node Q1 re-hardened flip-flop, state 1.

Figure 10 demonstrates that a resizing of the cell prevents a decrease of the node G1 voltage, enough to induce a bit flip of the Master. So, after the 600 ps upset duration, the high level of the node Q1 can be promptly restored. Figure 11 confirms the hardness improvement. The design adaptation, realized with the help of laser testing and electrical simulations, ameliorate significantly the SEU immunity of the hardened flip-flop.
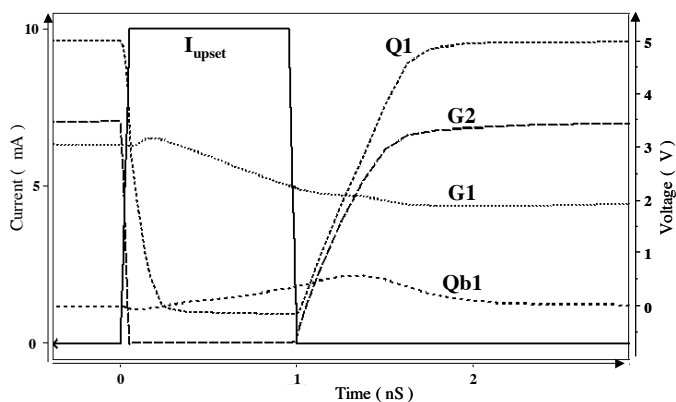

Fig. 11. Upset 900 ps 10 mA on node G2, re-hardened flip-flop, state 1.

VI. CONCLUSION

Laser testing of *circuit* can carry on the identification of some *configurations* propitious to the development of peculiar single event. To illustrate the purpose, we have presented a case not previously reported of a "back-generation" effect. This effect is related to an upset in a flip-flop. It leads to detect the presence of unattended soft errors in the memory cells of shift registers. A mapping allows us to intervene on the right element of the hardened circuit and to improve even

more its capabilities by resizing the design. This investigation shows relevant applications of the laser testing not only as a failure analysis instrument but also as a tool to improve the design rad hardening of the circuits.

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