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http://dx.doi.org/10.1109/IOLTS.2015.7229849
On-Line Testing Symposium (IOLTS), 2015 IEEE 21st International

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***Abstract*—Bulk Built-In Current Sensors (BBICS) were developed to detect the transient bulk currents induced in the bulk of integrated circuits when hit by ionizing particles or pulsed laser. This paper reports the experimental evaluation of a complete BBICS architecture, designed to simultaneously monitor PMOS and NMOS transistors, under Photoelectric Laser Stimulation (PLS). The obtained results are the first experimental proof of the efficiency of BBICS in laser fault injection detection attempts. Furthermore, this paper highlights the importance of BBICS tapping in a sensitive area (logical gates) for improved laser detection. It studies the performances of this BBICS architecture and suggests modifications for its future implementation.**

***Keywords*—Bulk Built-In Current Sensor, Hardware Security, Photoelectric Laser Stimulation, Single Event Effects, Laser Fault Injection, Countermeasures**

I. Introduction

When exposed to harsh environments in space, high atmosphere or even on Earth, integrated circuits (ICs) may undergo soft errors. The related phenomena are known and have been studied for more than forty years [1], [2], [3]. Among the various existing effects, single-event effects (SEEs) due to ionizing particles may result in a faulty behavior of the affected circuit. Since then, for the purpose of coping with the effects of such events, much research work has been devoted to the understanding and mitigation of SEEs. In this context, the use of pulsed lasers was introduced to emulate SEEs at the experimenter's bench [4], [5]. However, pulsed laser may also be used to induce faults (as a result of SEEs) into the computations of security-dedicated ICs for the purpose of retrieving the secret data they may contain [6], [7]. Fortunately, other techniques introduced by researchers in the radiation community to mitigate SEEs may be adapted to better cope with the issue of laser fault-injection. A fertile idea was the monitoring of the currents that happen with SEEs [8], [9]. This idea found its development in the principle of Bulk Built-In Current Sensors (BBICS) which were developed to detect transient currents induced in the bulk of ICs when hit by ionizing particles or a pulsed laser [10], [11].

This paper describes the principles underlying BBICS. It also introduces the architecture of the double-access BBICS. Only simple-access BBICS were, to date, once experimentally tested [12]. Based on this research, a new architecture has been implemented. Its weaknesses and strengths, revealed during the testing, are discussed below. Note that the reported work was done from a secure circuit point of view: we used laser pulse durations in the nanosecond range whereas a maximum pulse duration of a few tens of picoseconds should be used for emulating SEEs [5].

This paper is organized as follows: Section II describes the principle underlying BBICSs. The architecture of the double-access BBICS is introduced in Section III. The laser experiments of the single BBICS are described in Section IV. Its weaknesses and strengths, revealed during the testing of the test chip, are discussed. Then, Section V presents a conclusion.

II. State of the art

ICs are known to be impacted by SEEs caused by ionizing particles in radioactive environments. The related electrical phenomena and the detection principles using BBICSs are reviewed in the following subsections.

A. Single-Event Effects in Integrated Circuits

When an ionic particle passes through silicon it generates electron-hole pairs along its path. These electrical charges generally recombine without any significant effect on the IC computations. However the electric field found in reverse-biased PN junctions may separate the electron-hole pairs, inducing a parasitic transient current. This transient current may in turn disturb the voltage of the IC's internal nodes leading to computational errors. A pulsed laser may be used to mimic (or emulate) this phenomenon provided that its photons energy is greater than the silicon bandgap (electron-hole pairs are then induced by photoelectric effect [4], [5]). At first, pulsed lasers were used to emulate SEE generation in ICs for radiation hardness evaluation. Since then, they are also used to induce faults into secure circuits for the purpose of retrieving confidential data stored into that devices [6], [7]. The following describes laser-induced SEEs and the principles of their detection by BBICS. A laser-induced transient current is then called a '*photocurrent*' [13], [14], [15], [16].

The way a transient photocurrent is turned into a SEE is illustrated in Fig. 1 for the inverter case when its input is at

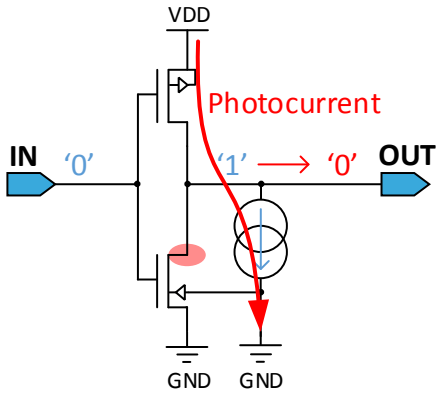

Fig. 1. Laser-sensitive area of a CMOS inverter with its input at low level

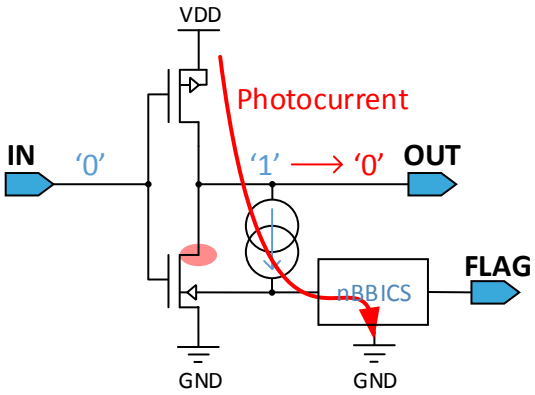

Fig. 2. Principle of SEE detection by a NMOS dedicated nBBICS

low logical level. In this configuration, the SEE sensitive area is the drain of the NMOS transistor (shaded in pink), which is in OFF state. A laser-induced photocurrent, depicted by a current source in Fig. 1, may be injected there through the reverse-biased PN junction between the N-type drain of the NMOS (biased at VDD) and the P-type substrate (grounded). As a result of the latter, the inverter output voltage may drop from '1' to '0' provided that the injected photocurrent is higher than the PMOS transistor saturation current. This voltage transient, also known as SET (Single Event Transient), may thus propagate through the circuit logic, creating errors. Furthermore, if a SET is induced directly in a memory element, as a latch, the stored data may be flipped, characterizing the so-called SEU (Single Event Upset; i.e. a bit set from '0' to '1' or a bit reset from '1' to '0'). Note that a similar phenomenon may also take place when the inverter input is at a high logical state (in this instance the laser-sensitive place is the drain of the OFF PMOS): the photocurrent then flows from VDD through the biasing contact (or tap) of the Nwell (i.e. the PMOS bulk) to ground. An interesting feature of such SEE transient currents is that they flow through the bulk of the sensitive transistors.

B. BBICS *principles*

Bulk currents induced during the normal operation of an IC are in the µA range; whereas particle- or laser-induced bulk currents have to be above two orders of magnitude to generate an SET on the related gate output [10]. BBICSs are designed to take advantage of this property; they monitor bulk currents, hence they are able to detect unusual currents and, consequently, the advent of SEE [17], [18], [19]. Fig. 2 depicts the insertion of a BBICS between the bulk (i.e. the Psubstrate) of NMOS transistors and the ground. Hence, as illustrated, any transient photocurrent necessarily flows through the BBICS. The purpose of the BBICS is then to raise a warning flag indicating that the circuit function may be affected. Note that the BBICS has also to provide the biasing of the transistor's bulk, a ground biasing in case of NMOS. In Fig. 2, the BBICS used to monitor NMOS transistors is named nBBICS. There also exists pBBICS dedicated to the monitoring of PMOS transistors. Even if pBBICS and nBBICS have different architectures they rely on the same principle, i.e. the monitoring of bulk currents.

Among various BBICS architecture proposals [11], [20], [18], only one was, to date, experimentally tested [12]. The authors designed both NMOS- and PMOS-BIVS (Built-In Voltage Sensor according to the authors' denomination) to monitor NMOS and PMOS.

C. BBICS *experimental validation*

Most of the research was based on simulations [8], [21], [20], [22], [23], [24]. The only experimental tests was investigated with a $1\,ps$ laser source with a $800\,nm$ wavelength and a $1.6\,\mu m$ spot size diameter. Their paper proves that a NMOS-BIVS standalone is less sensitive than PMOS-BIVS. The sensitivity threshold for NMOS-BIVS is $110\,pJ$ whereas it is only $15\,pJ$ for PMOS-BIVS (results with 10 contacts to the sensors)[12]. Our evaluations are dedicated to improve the efficiency of the sensor by merging both NMOS- and PMOS-BIVS. Futhermore our investigations will provide spatial information of the sensitivity detection regarding the tapping of the target.

III. Architecture of the single BBICS used in the experiments

A. BBICS *architecture*

Fig. 3 depicts the architecture of the BBICS we designed and used for practical validation with a laser. Its main feature is its ability to simultaneously monitor NMOS and PMOS transistors. Two cross-coupled inverters are used to store the content of a warning flag: OUT node. OUT goes to high level to indicate the detection of any unusual bulk current, and stays low in monitoring mode. The INNWELL and INPWELL nodes are the respective BBICS connections to the biasing contacts of the PMOS and NMOS bulks. Transistors MP1 and MN1 are used to bias the INNWELL and INPWELL nodes, respectively, at VDD and ground. In this way, they ensure the proper biasing of the corresponding bulk. These transistors are always in ON state. The purpose of transistor MP2 and MN2, whose drains are connected to the OUTB and OUTA nodes, is to raise the alarm flag in case of the advent of a SEE according to the process explained below. The single BBICS architecture also has a reset mechanism (RESET input) thanks to transistors MP3 and MN3. Finally an inverter and an OR2 gate inserted between OUTA and OUTB nodes make it possible to aggregate

several alarm flags into a single one by using the INSENSOR input.

When a bulk current is induced by the laser, OUTA and OUTB change their stable state in the latch, so consequently, the output of the sensor (OUT) is at '1'. The latch has to be very sensitive to be able to detect small variations of their input voltage. The latch memorizes a state if there was a transient bulk current, so it needs to be reset at every acquisition.

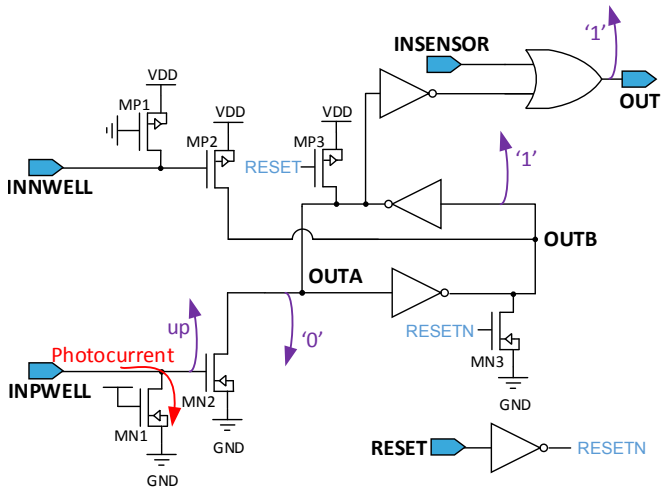

Fig. 3. Single BBICS architecture and principle of SEE detection

Fig. 3 also highlights (in purple) the chain of events involved in bulk current detection by the single BBICS. Consider the case of a radiative- or laser-induced SEE targeting a NMOS monitored by the single BBICS: a bulk current will flow through transistor MN1 in order to reach ground (the red arrow denoted '*Photocurrent*' in Fig. 3). As a result the voltage at INPWELL node will rise (denoted '*up*') causing the MN2 transistor to switch from the OFF to the ON state, hence connecting node OUTA to ground. Then node OUTB will go to high level latching the BBICS in alarm mode. The alarm flag OUT will also go to a high logical level revealing the induction of a bulk current. A similar behavior takes place (due to transistors MP1 and MP2) for bulk currents related to PMOS transistors.

B. Device under test

Our target, or device under test (DUT), was designed in the $90\,nm$ STMicroelectronics CMOS technology (its core voltage is $1.2\,V$). We focused our study on the area of a purely combinational logic block monitored by a single BBICS.

To understand the different detection maps reported in Section IV, Fig. 4 describes how the blocks are distributed in the layout. The monitored area is $14\,\mu m$ from the BBICS to avoid any perturbation during acquisitions. The laser detection maps will cover both the monitored area and the BBICS ($80\,\mu m \times 60\,\mu m$ with a step size of $1\,\mu m$).

As stated previously, a BBICS is also in charge of providing the substrate and well biasing of the logic it monitors. In our design, we chose to provide this biasing through the BBICS as well as through the IC's power/ground network (PGN). Our

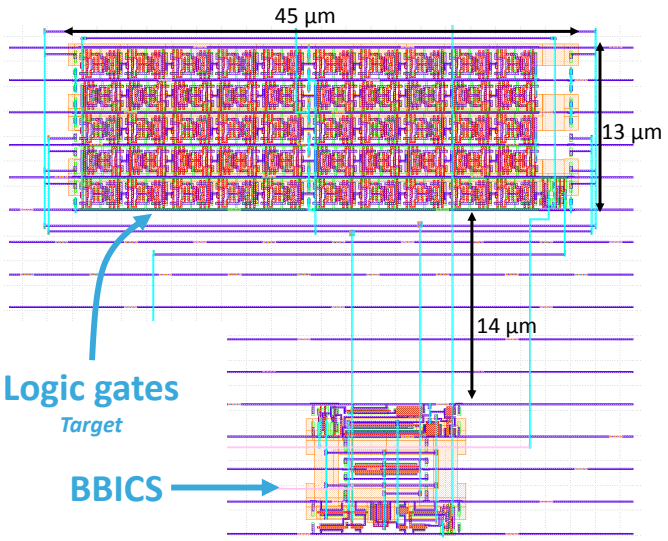

Fig. 4. Area of interest: layout of the single BBICS and of the logic gates it monitors

intent was to test the BBICS efficiency while maintaining a proper biasing through the PGN (Psubstrate at Gnd and Nwell at VDD) even in the case of an induced SEE current (and thus modifying the biasing provided by the BBICS). Fig. 5 displays the bias tapping of the monitored logic: the Psubstrate biasing contacts to ground (or bias tapping) are designated by either Ptap for a BBICS provided bias or GND for a PGN bias. The Nwell biasing ($1.2\,V$) contacts are denoted by either Ntap for a BBICS provided bias or VDD for a PGN bias. For the sake of readability, Fig. 5 only displays the Nwell layer of the logic gates layout.

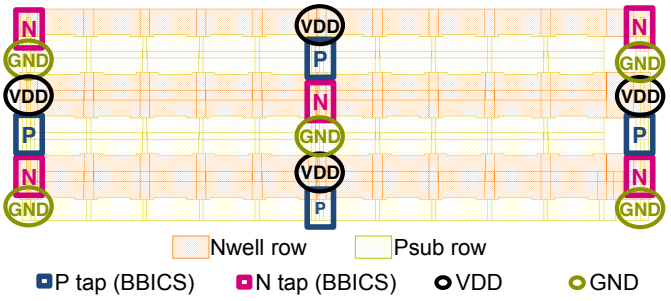

Fig. 5. Details of the well taps and BBICS taps of the target

The cells of the monitored logic gates are located on the three Nwell and three Psubstrate rows highlighted in Fig. 5. Classical well taps are alternated with BBICS taps every $25\,\mu m$. That tapping can be called an hybrid tapping or a 50% BBICS tapping because it merges classical well tapping at the power supply and BBICS tapping.

However, such hybrid taping may weaken the BBICS efficiency in detecting laser-induced bulk currents as illustrated in Fig. 6. Indeed, the photocurrents flowing from VDD to ground may follow two paths: one through the BBICS taps and the other to or from the PGN. The thicker arrow indicates the less resistive path for the photocurrent. The photocurrent will choose preferentially this less resistive path: so, depending on

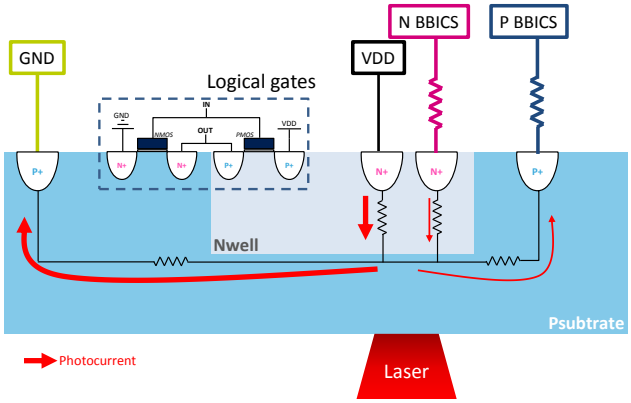

Fig. 6. Cross sectional view of a BBICS monitored logical gate with photocurrent paths

the position of the laser spot (w.r.t. the biasing contacts), the photocurrent may flow partly through the PGN or the BBICS taps according to the resistivity of these two paths. As a result, the laser-induced bulk current flowing through the BBICS may be reduced, hence lowering its SEE detecting ability. Our test chip was designed to test experimentally this phenomenon.

IV. Experiments

A. Experimental set-up

The laser source we used during our experiments produces laser pulses in the nanosecond range (it was set to $200\,ns$, $100\,ns$ or $50\,ns$ pulse duration for the test series we reported in this paper). It has a $1064\,nm$ wavelength (near IR), which makes it possible to access the sensitive areas of a target through its backside (i.e. through its silicon substrate). Our tests were actually performed through the target backside, which was thinned to $\sim 150\,\mu m$ thickness to minimize the amount of power lost along the laser beam path. The laser beam was focused on the DUT's sensitive parts: given the $\times 100$ optic we used, we obtained a laser spot with a diameter of $\sim 1\,\mu m$ (refer to [5] for a complete description of laser beam propagation through silicon and beam focusing). Three laser pulse durations and two laser powers were chosen to have a full coverage area and evaluate the sensitivy map for lower laser pulse duration and lower laser power. Detection maps were drawn to have a spatial representation of the BBICS area of detection.

To plot the sensitivity maps (i.e. the XY coordinates at which a laser shot make the BBICS alarm flag to rise), the laser moves thanks to a XYZ stage (accurate to $0.1\,\mu m$) whereas the wafer is fixed. At every point, all the input signals are set with an FPGA, and the acquisitions are captured by a remote oscilloscope.

The laser is shot when the reset signal is stable, the acquisition of the output needs to be done after a delay. Indeed, the BBICS will flag after a delay because of the capacitor (and resistivity) of the net and the gate delay. It depends also on the layout topology. In our case, the detection response is after a few nanoseconds.

For our experiments, the main objective was to understand double-access BBICS detection, with the BBICS plugged in a sensitive area (logical gates) with different well taps and different BBICS taps (see Fig. 5).

B. Evaluation at $300\,mW$ laser power (BBICS sensitivity maps)

The first detection (or sensitivity) maps at $300\,mW$ laser power (Fig. 7a, Fig. 7b and Fig. 7c) show that the sensitive area is fully covered at $200\,ns$ but exhibits some hidden areas at $100\,ns$ and $50\,ns$. In Fig. 7b the Gnd and VDD power supply taps hide part of the detection area. This is because the photocurrent generated close to these taps chooses the less resistive path and this path is the Gnd or VDD power supply taps path compared to the BBICS taps. So the BBICS does not flag close to Gnd and VDD taps.

In Fig. 7c, some detection areas are missing, those ones close to BBICS taps (N and P standalone). The couple of P and N BBICS taps detect more than only one BBICS taps. This can be explained by the latch inside the BBICS which is toggled on the two sides close to the couple P and N BBICS taps and on only one side close the N or P BBICS taps. The more there are BBICS taps, the more effective the detection is.

A detection area is also present in the BBICS itself. It is not due to the photocurrent in the BBICS taps, but to an SEU in the latch of the BBICS. Indeed a latch changes states from '0' to '1' when the laser is close to sensitive junction of the inverters [15].

C. Evaluation at $250\,mW$ laser power (BBICS sensitivity and photocurrent maps)

The second detection maps at $250\,mW$ (Fig. 7d, Fig. 7e and Fig. 7f) confirm the trend in the previous detection maps. Their coverage is smaller than the previous ones because the photocurrent is reduced (the photocurrent depends on the laser power). These detection maps confirm that the sensitive area is hidden because of the Gnd and VDD power supply taps compared to the BBICS taps. The detection areas are localized close to the BBICS taps but precisely close to the couple of P and N BBICS taps. Indeed close to the single P and N BBICS taps there is not any detection in Fig. 7e and Fig. 7f, for example in the upper corners. The couple P and N BBICS are more effective than single taps. This can be explained because the latch in the design is toggled on both sides. The more there are BBICS taps, the more effective the detection is.

A detection area is also present in the BBICS itself. As in the IV-B, detection does not occur because of the photocurrent in the BBICS taps but because of the SEU in the latch of the BBICS. Indeed a latch will change states from '0' to '1' when the laser is close to the sensitive junction of the inverters.

As well as drawing BBICS detection maps, we also measured the laser-induced photocurrents at $0.25\,W$ laser power. Fig. 8 displays maps of the magnitude of the transient photocurrent pulses obtained at $100\,ns$ (Fig. 8a) or $50\,ns$ (Fig. 8b) laser pulse duration: the maximum current magnitude is given according a color scale for each location (XY coordinates) of the laser shots on the BBICS monitored part of the DUT. Given practical issues of the test bench, Fig. 8 reports the magnitude of the whole photocurrent flowing through the ground connection of the DUT: i.e. the sum of two photocurrents components

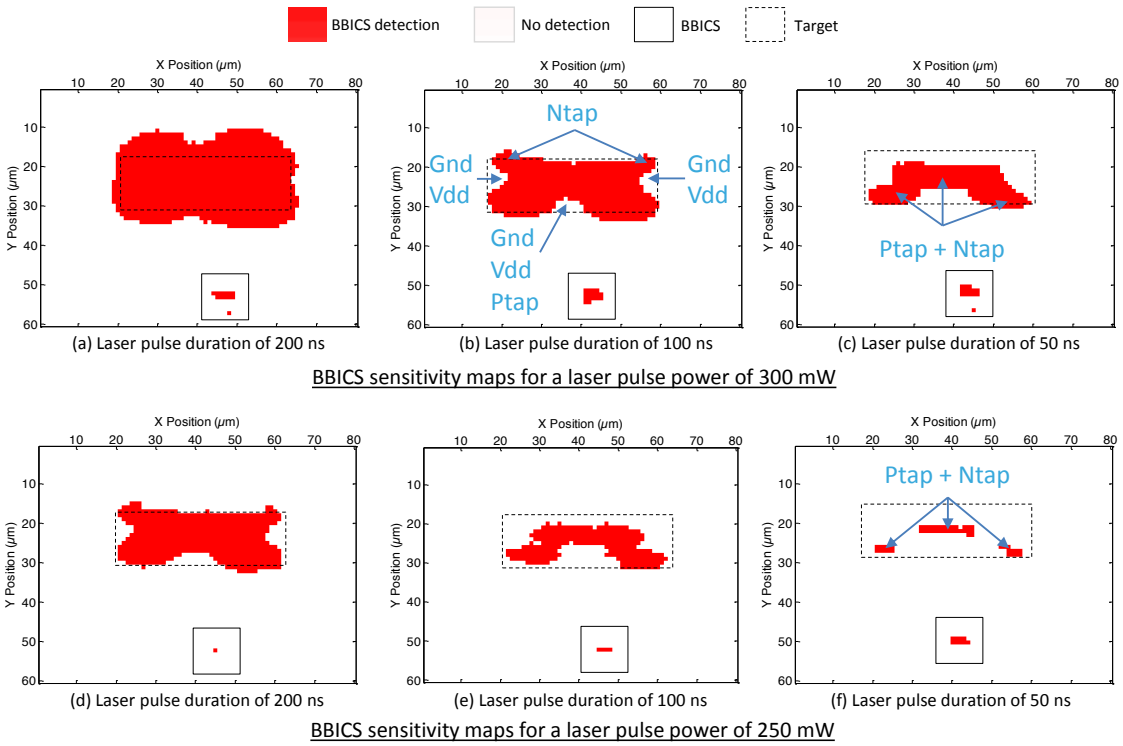

Fig. 7. BBICS laser detection at $0.3\,W$ and $0.25\,W$ and for a laser pulse duration of $200\,ns$, $100\,ns$ and $50\,ns$

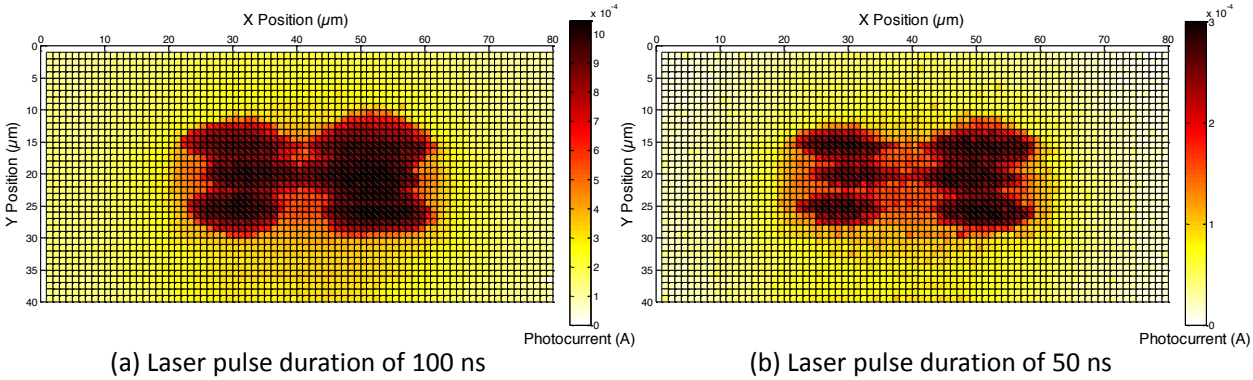

Fig. 8. Laser-induced map of the photocurrent flowing through the test chip ground connection for $100\,ns$ and $50\,ns$ pulse duration at $0.25\,W$

flowing (1) through the PGN GND tap and (2) the BBICS Ptap connections (marked respectively GND and P BBICS in Fig. 6). Hence, we were not able to measure the individual values of these two components. The shapes of the three Nwells of the monitored logic (see Fig. 5) are clearly visible: they correspond to the highest magnitude of the laser-induced photocurrents. At $100\,ns$ laser pulse duration and $0.25\,W$ laser power a maximum photocurrent magnitude of $1.2\,mA$ was obtained. The maximum photocurrent magnitude is only $300\,\mu A$ at $50\,ns$ laser pulse duration for the same laser power. The shape of the Nwell is also more precisely drawn at $50\,ns$. This is no surprise that a photocurrent map reveals the Nwells because they are the place where the biggest reverse-biased PN junctions of the device are.

It has been proven that the photocurrent is higher on Nwell/Psub junctions compared to MOS/Wells junctions (N+/Psub or Nwell/P+) [15], [14], [16]. To conclude, these photocurrent maps allow us to estimate of the BBICS limit threshold. The reader will also notice that the middle part of each Nwell exhibits a photocurrent magnitude lower than at its right and left ends. We have not yet a valid explanation of this phenomenon. These measures provide a broad idea of the photocurrent that may be detected by the single BBICS.

D. Results analysis

The BBICS detection threshold can be tuned by changing the W/L ratio of MN1 and MP1 transistors. The more resitive these transitors are, the more effective the detection at low photocurrent is; but if the MOS are too resistive, the BBICS will

not detect very short pulses. So the design needs to consider those two aspects to perfectly tune the BBICS.

The efficiency of the detection is low close to Gnd/VDD taps because there is not enough transient current for the BBICS. A Ptap and Ntap standalone close to Gnd/VDD also present weakness described by [12]. Only one access is not adequate for a good detection: this validates the single BBICS design which uses two accesses respectively to the Psubstrate and to the Nwells.

Some parts of the monitored logic gates are not covered by the sensors whereas some SEU are present in the BBICS itself. It proves that these laser settings may disturb the behavior of an IC without being detected. The use of an hybrid well-taping seems to be the root cause of this weakness because it reduces the laser-induced bulk current flowing through the BBICS. Our experiments underline the efficiency of a BBICS architecture that collects SEE currents from both the Psubstrate and Nwells.

V. Conclusion

The architecture of this single BBICS demonstrated that the detection is very effective for long laser pulse durations close to P and N taps couples but may fail for short pulses. Furthermore, this distributed tapping allows us to think that a full BBICS tapping will enhance the sensitive detection area (the more there are BBICS taps, the more effective the detection is). If the resistive MOS transistors in the circuit are too resistive, the BBICS will not detect very short pulses but they will permit to detect low photocurrents. So the design needs to consider these two aspects to perfectly tune the BBICS. In order to validate this hypothesis, new BBICS will be tested with different well tapping (100% BBICS taps), different spacing between the taps and different resistive MOS in the circuit, to ameliorate the coverage detection. Finally, picosecond range laser evaluations will be done on these structures, for the radiation field, in order to have a complete evaluation of the double access BBICS.

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