# SEU sensitivity and modeling using pico-second pulsed laser stimulation of a D Flip-Flop in 40 nm CMOS technology

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# Electrical modeling of a picosecond pulsed photoelectric laser stimulation on a D Flip-Flop in 40 nm technology

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***Abstract*—This paper presents the design of D Flip-Flop cell and reports the laser fault sensitivity mapping both with experiments and simulation results. Theses studies are driven by the need to propose a simulation methodology based on laser/silicon interactions with a complex integrated circuit. In the security field, it is therefore mandatory to understand the behavior of sensible devices like D Flip-Flops to laser stimulation. In previous works, Roscian et al., Sarafianos et al., Lacruche et al. or Courbon et al. studied the relations between the layout of cells, its different laser-sensitive areas and their associated fault model using laser pulse duration in the nanosecond range. In this paper, we report similar experiments carried out using shorter laser pulse duration (30 ps instead of 50 ns). We also propose an upgrade of the simulation model they used to take into account laser pulse durations in the picosecond range on a logic gate composed by a large number of transistors for a recent CMOS technology (40 nm).**

***Keywords*—*D Flip-Flop cell, Hardware Security, Photoelectric Laser Stimulation, Single Event Effects, Laser Fault Injection, Electrical Modeling***

## I. Introduction

When exposed to an harsh environment in space, high atmosphere or even on earth, integrated circuits (ICs) may undergo soft errors. The related phenomenons are known and studied for more than forty years [1–3]. Among the various existing phenomenon, single event effects (SEEs) due to ionizing particles may result in a faulty behavior of the hit circuit. Since then, for the purpose of coping with the effects of such events, a lot of research work is devoted to the understanding and mitigating of SEEs. In this context, the use of pulsed-lasers was introduced to emulate SEEs [4], [5]. However, pulsed-laser may also be used to induced faults (as a result of SEEs) into the computations of security-dedicated ICs for the purpose of retrieving the secret data they may contain [6], [7]. Fortunately, other techniques introduced by researchers of the radiation community to mitigate SEEs may be adapt to cope with the issue of laser fault-injection. Electrical models have been created in order to propose a fast and simulated analysis (SPICE) of a circuit under laser stimulation. These electrical models make it possible to simulate the response of integrated circuit to laser pulses in a very small amount of calculation time by comparison with physical experiments on laser equipment or TCAD simulation. The novelty of this paper is that our model takes into account very short laser pulses duration with a thin spatial accuracy to identify sensitive areas for a recent CMOS technology ($40\,nm$ instead of $0.25\,\mu m$ or $90\,nm$).

This paper is organized as follows: Section II describes the principles of laser fault injection. The architecture of D Flip-Flop used in our experiments is introduced in Section III. Hypothesis are made and validated both with experiments (Section IV) and modeling (Section V). Weaknesses and strengths, revealed during the testing, are discussed afterward. Note that the reported work was done from a secure circuit point of view. We used laser pulse duration in the picosecond range for emulating SEEs [5]. Then, Section VI draws a conclusion.

## II. State of the art

ICs are known to be impacted by SEEs caused by ionizing particles in radioactive environments. The related electrical phenomenon and the laser impacts on gates, as latch, SRAM (Static Random Access Memory) or D Flip-Flop, are reviewed in the following subsections.

### A. Single Event Effects in Integrated Circuits

When an ionic particle passes through silicon, it generates electron-hole pairs along its path. These electrical charges generally recombine without any significant effect on the IC computations. However the electric field found in reverse-biased PN junctions may separate the electron-hole pairs, inducing a parasitic transient current. This transient current may in turn disturb the voltage of the IC's internal nodes leading to computational errors. A pulsed laser may be used to mimic (or emulate) this phenomenon provided that its photons energy is bigger than the silicon bandgap (electron-hole pairs are then induced by photoelectric effect [4], [5]). At first, pulsed lasers were used to emulate SEE generation in ICs

for radiation hardness evaluation. Since then, they are also used to induce faults into secure circuits for the purpose of retrieving confidential data stored into that devices [6], [7]. In the following, laser-induced SEEs is described. A laser-induced transient current is then called a '*photocurrent*' [8–16].

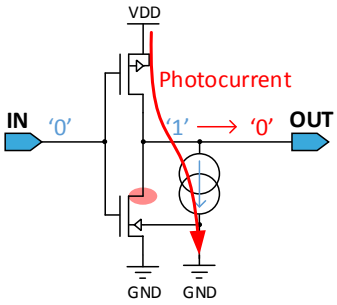


Fig. 1. Laser-sensitive area of a CMOS inverter with its input at low level

The way how a transient photocurrent is turned into a SEE is illustrated in Fig. 1 for the inverter case when its input is at low logical level. In this configuration, the SEE sensitive area is the drain of the NMOS transistor (shaded in pink), which is in OFF state. A laser-induced photocurrent, depicted by a current source in Fig. 1, may be injected there through the reverse-biased PN junction between the N-type drain of the NMOS (biased at VDD) and the P-type substrate (grounded). As a result of the latter, the inverter output voltage may drop from '1' to '0' provided that the injected photocurrent is higher than the PMOS transistor saturation current. This voltage transient, also known as SET (Single Event Transient), may thus propagate through the circuit logic, creating errors. Furthermore, if a SET is induced directly in a memory element, as a latch, the stored data may be flipped, characterizing the so-called SEU (Single Event Upset; i.e. a bit set from '0' to '1' or a bit reset from '1' to '0').

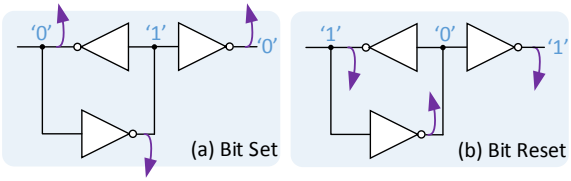


Fig. 2. Single Event Upset (SEU) description on a latch

Fig. 2 shows the behavior of a latch when a SEU is induced. The increasing or decreasing potential of nodes are symbolized by the purples arrows. If the arrow is oriented to the top the potential increase from '0' to '1' whereas if the arrow is oriented to the bottom the potential decrease from '1' to '0'. Note that a similar phenomenon may also take place when the inverter input is at a high logical state (in this instance the laser-sensitive place is the drain of the OFF PMOS): the photocurrent then flows from VDD through the biasing contact (or tap) of the Nwell (i.e. the PMOS bulk) to ground.

### *B. D Flip-Flop principles*

In a secure integrated circuit, a D Flip-Flop is a fundamental element in order to store information or many other uses. An important number of basic Flip-flops cells (more than thousands) can be implemented in circuits, so the protection of these cells become mandatory to thwart laser attacks (it has been revealed that a D Flip-Flop is a security weakness point). Our studies on this basic cell will permit to fine tune the photoelectric model in order to evaluate more complex circuits.

A D Flip-Flop is a memory cell, which memorizes a data in an electronic circuit following the truth table in TABLE I. This cell functions regarding a clock signal. At rising edge on the clock signal, the data in the input of the cell will be in the output but the particularity is to memorize the state when the clock signal is at '0' (non rising).

| CLK | D | $Q_{next}$ | Comments |
|---|---|---|---|
| Rising Edge | 0 | 0 | $Q_{next} = D = 0$ |
| Rising Edge | 1 | 1 | $Q_{next} = D = 1$ |
| Non Rising | X | Q | Memorizing |

TABLE I. TRUTH TABLE OF THE D FLIP-FLOP

### *C. Memory cells under pulsed photoelectrical laser stimulation*

Roscian et al. [9], Sarafianos et al. [8], [12] and Lacruche et al. [16] describes the laser sensitivity of SRAM cells. They also develop an effective model for laser pulse durations above $50\,ns$. Theirs researches permit to identify the critical junctions in a circuit and the importance of the topology (layout) with an old CMOS technology ($0.25\,\mu m$) and a low spatial resolution. Indeed, long laser pulse durations have not permitted to identify precisely the sensitive areas (one area was hidden both with experiments and model). Roscian et al. [9] proved that a $1\,\mu m$ spot size was perfect to characterize accurately the sensitive areas. On the other hand, Courbon et al. [17] led his researches on SEU on D Flip-Flop laser sensitivity but without controlling the clock signal an so without impacting the master latch. He demonstrates that he was able to obtain one failure mode by reducing the laser power. Unfortunately the layout recognition was not communicated and the sensitivity junctions was not identified precisely. Indeed the step size of the maps they chose was too high compared to the size of transistors to identify a large amont of gates in his circuit but they are able to identify Flip-Flops and their orientation in a glue logic. In previous works, Lacruche et al. [16] ameliorated the electrical model for picosecond laser pulses based on a comparison of a $50\,ns$ ans a $30\,ps$ laser pulse duration of fault on a SRAM cell in $0.25\,\mu m$ CMOS technology. It has been shown that with a picosecond source the sensitive area are more distinguishable than with nanosecond source. Considering their works, we chose to perform accurate maps in order to reveal precisely the sensitive areas choosing a thin spot size and a picosecond source on a recent CMOS technology circuit ($40\,nm$).

To control laser impacts either on master latch or slave latch, the input signals must be perfectly set as it is explained in Fig. 3 and Fig. 4. First at CLK='0' the data is not yet in the master latch, it will be transferred and memorized at the rising edge. If CLK stays at '1', the impacted latch is the master one

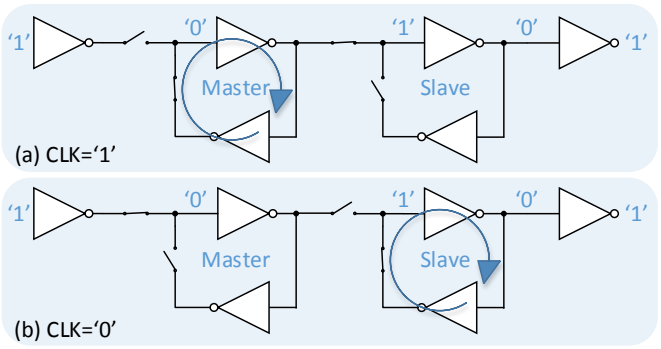


Fig. 3. Flip-Flop settings with input at '1' in order to impact either Master latch or Slave latch

(Fig. 3a and Fig. 4a) but if the CLK goes back to '0' the data will be transferred and memorized in the slave latch (Fig. 3b and Fig. 4b).

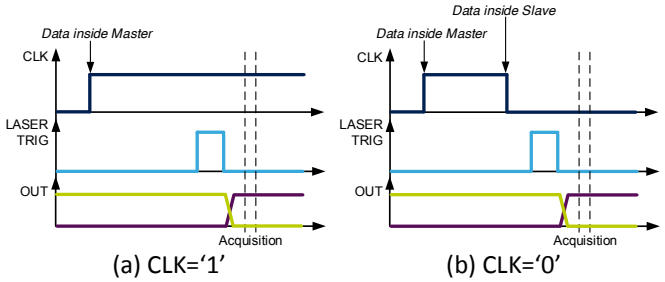


Fig. 4. Timing diagrams of the different configurations of the D Flip-Flop

## III. Architecture of the D Flip-Flop used in the experiments

### A. D Flip-Flop architecture

The cell studied in this section of the paper is a D Flip-Flop made of 24 transistors similar to those used in secure integrated circuits (Fig. 6) and based on a basic architecture using two latches : a master latch and a slave one (Fig. 3). There is no reset in that structure in order to simplify the studies by minimizing the number of transistors. Indeed basically a D Flip-Flop requires several stages: inverting input buffers, two latches, output buffers, clock inverters and asynchronous reset signal. Note that this standalone Flip-flop is embedded in a test chip designed in a CMOS $40\,nm$ process.

### B. Theoretical photoelectric sensitive junctions

In the D Flip-Flop, the fault areas are separated in two parts: master latch and slave latch. The settings for those both parts are reminded in Fig. 3 depending on the input signals (Fig. 4). In this subsection, the D Flip-Flop cell sensitivity is studied from a theoretical point of view (considering its schematic and its state).

In order to simplify the explanation, the theoretical photoelectric sensitive junctions are described on a simple latch. Obviously it is similar for both latches composing the D Flip-Flop. Two cases are considered: input at '0' and input at '1'.

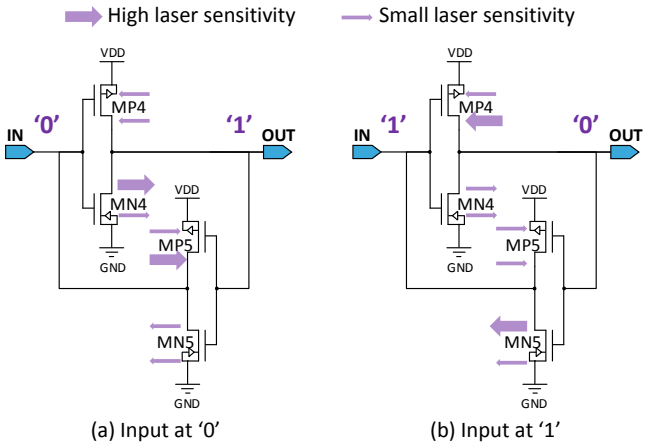


Fig. 5. Schematic of a latch cell laser sensitivity with input at '0' and '1'

*1) Input at '0':* When the input is at '0', the OUT node is at '1'. Based on [8], [9], [12], [16], [18], the sensitivity of the cell can be investigated by considering which PN junctions are the most reverse biased in function of the latch state. Indeed, these reverse biased PN junctions are the place where the electrical field is strong enough to generate a transient current likely to induce an SEU. It is well known than more the PN junction is reversed biased more the photocurrent generated is. Based on this fact, we show the direction and photocurrent ratio on Fig. 5a. The purple arrows give the directions of the induced photocurrents between the transistors Drain and bulk or Source and bulk. The thick arrows represent strong photocurrents, the thin arrows smaller ones. The junctions where the photocurrent is the more important are the most sensitive.

Consequently, in Fig. 5a, the two most sensitive areas to laser illumination are the drain junctions of MN4 and MP5 transistors.

*2) Input at '1':* When the input is at '1', the OUT node is at '0'. Based on same investigations, the direction and photocurrent ratio are depicted on Fig. 5b. Consequently, the two most sensitive areas to laser illumination are the drain junctions of MP4 and MN5 transistors.

Therefore, four sensitive areas are expected on the latch: two with the input at '0' and two others with input at '1'.

According to the previous paragraphs, fourteen photoelectrical sensitive junctions on the D Flip-Flop can be identified, on the schematics and layout (Fig. 6 and Fig. 7), eight on latches and six on pass gates. The blue circles are the areas where the laser injection changes the data from '1' to '0' (the bit reset) whereas the red circles are the areas where the laser injection changes the data from '0' to '1' (the bit set).

## IV. Experiments

### A. Device under test

The device under test (DUT), was designed in the $40\,nm$ STMicroelectronics CMOS technology and its core voltage is $1.2\,V$.

To understand the different detection maps reported in section IV-C, Fig. 7 describes how the transistors are distributed

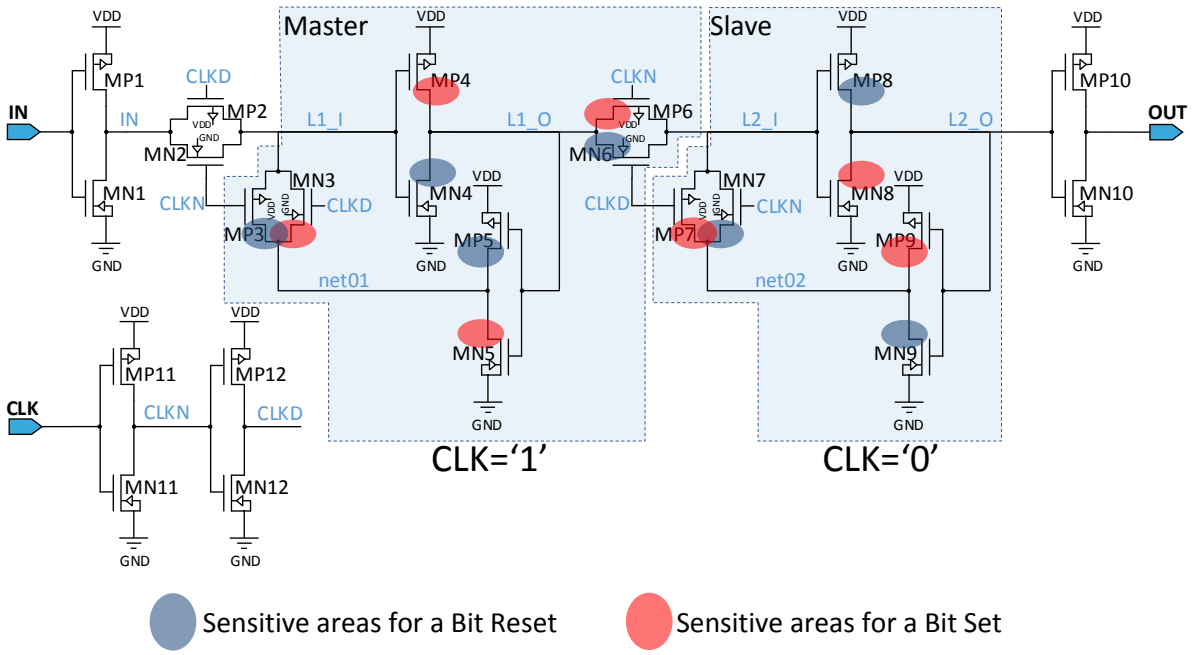


Fig. 6. D Flip-Flop architecture with theoretical photoelectric sensitive junctions

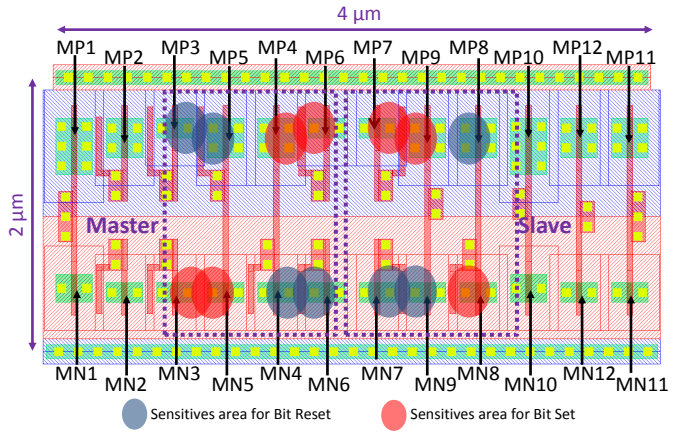


Fig. 7. Layout of the D Flip-Flop with theoretical photoelectric sensitive junctions with each transitors referenced

in the layout. The laser maps will cover the D Flip-Flop ($10\,\mu m \times 6\,\mu m$ with a step size of $0.2\,\mu m$) on a test chip.

### B. Experimental set-up

The laser source used during the experiments produces laser pulses in the picosecond range (it was set to $30\,ps$ pulse duration for the test series we reported in this paper). It has a $1030\,nm$ wavelength (near Infra-Red), which makes it possible to access to the sensitive areas of a target through its backside (i.e. through its silicon substrate). Our tests were actually performed through the target backside, which was thinned to $\sim 150\,\mu m$ thickness to minimize the amount of power lost along the laser beam path due to the absorption phenomena. The laser beam was focused on the DUT's sensitive parts: given the $\times 100$ optic we used, we obtained a laser spot with a diameter of $\sim 1\,\mu m$ (refer to [5] for a complete description of laser beam propagation through silicon and beam focusing). Fault maps were drawn to have a spatial representation of the area of faults.

To plot the sensitivity maps, the laser moves thanks to a XYZ stage (accurate to $0.1\,\mu m$) whereas the test chip is fixed. At every points, all the input signal are set with an FPGA, and the acquisitions are captured by a remote oscilloscope.

The experiments are divided in four steps depending on Fig. 4, these four cases are developed in TABLE II. Then the four result are merged in only one maps to simplify the visualization and understanding.

| Steps number | Input (D) | Clock (CLK) | Comments |
|---|---|---|---|
| Step 1 | 0 | 0 | Bit set in slave latch |
| Step 2 | 0 | 1 | Bit set in master latch |
| Step 3 | 1 | 0 | Bit reset in slave latch |
| Step 4 | 1 | 1 | Bit reset in master latch |

TABLE II. TABLE OF D FLIP-FLOP EXPERIMENTAL STEPS

The laser is shot when all signals are stable (Fig. 3 and Fig. 4). The acquisition of the output needs to be done after a delay. Indeed, the D Flip-Flop will change its state after a delay because of the capacitor (and resistivity) of the net and the gate delay. It depends also on the layout topology. In our case, the response is after a few nanoseconds.

For our experiments, the main objective was to understand the sensitivity maps in order to enhance the electrical model of pulsed PLS.

### C. Evaluation at $0.7\,nJ$ laser energy (SEU sensitivity maps)

The experimental fault (or sensitivity) map at $0.7\,nJ$ laser energy is given in Fig. 8. It shows that the sensitive areas are the same as the photoelectrical hypothesis ones but exhibits

| Transistors | Ratio W/L | Comments |
|---|---|---|
| MN1, MN10 | 5 | NMOS BUF/INV |
| MN2, MN3, MN6, MN7 | 3.5 | NMOS Pass gates |
| MN4, MN5, MN8 MN9, MN11, MN12 | 3.5 | NMOS INV |
| MP1, MP10 | 10 | PMOS BUF/INV |
| MP2, MP3, MP6, MP7 | 3.5 | PMOS Pass gates |
| MP4, MP5, MP8 MP9, MP11, MP12 | 7 | PMOS INV |

TABLE III. DESCRIPTION TABLE OF TRANSISTORS SIZE RATIO

one hidden areas. This hidden area can be explained because of the capacitor on L2_O node. Indeed the capacitors Gate-Bulk of the transitors of the Buffer/Inverter are bigger than the inverters in the latch (TABLE III). Also there is no common junction with a pass gate on MN8 transistor so it needs more energy for this area to appear. A common junction shared with two transistors is more sensitive than only one junction.

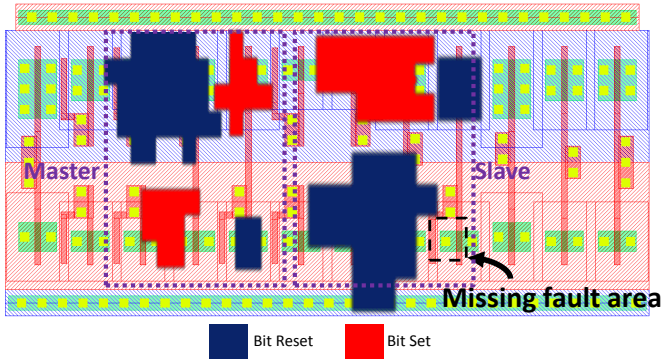


Fig. 8. Experimental results of a photoelectrical laser stimulation on a D Flip-Flop with a laser pulse duration of $30\,ps$ and a laser energy of $0.7\,nJ$

## V. ELECTRICAL MODELING OF THE PULSED PLS

The photocurrent generated by a pulsed-laser in an IC, are generally modeled by current sources plugged in parallel to its PN junctions. The electrical models under pulsed laser stimulation (N+ on Psubstrate, P+ on Nwell and Nwell on Psubstrate) were previously introduced [10], [11], [13], [15]. We have also already published electrical models, based on these preliminary studies made from measurements and simulations, on basic structures, which create photoelectrical effects. These models consist in a current source controlled by voltage to model the laser induced photocurrent. These models take into accounts the laser's spot size, power, pulse duration, focus of the laser beam and spatial parameters (location, geometry, wafer thickness). This is the first electrical stimulation test compared to measurements of a relatively complex CMOS cell in $40\,nm$.

### A. PN *junction modeling*

Using the laser beams to study each junction of our structure lets us create PN junctions models (called Subckt_Iph_diode) which contain a voltage-controlled current source. The amplitude value of this current source is defined by $I_{ph}$ as expressed in Eq. 1:

$$I_{ph} = \frac{1}{\gamma}(\alpha V + b)\alpha_{gauss} Pulse_{width} W_{coef} I_{ph\_z} \quad (1)$$

where, $V$ is the reverse biased voltage, $a$ and $b$ depend on the laser power, $\gamma$ is an amplitude attenuation coefficient, $\alpha_{gauss}$ is the sum of two Gaussian functions which take into account the spatial dependency, $Pulse_{width}$ considers the laser pulse duration dependency, $W_{coef}$ is an exponential function allowing for the wafer thickness effect and $I_{ph\_z}$ is a curve function which considers the focus effect of the z axis of the laser lens:

$$\alpha_{gauss} = \beta e^{\frac{-d^2}{c_1}} + \rho e^{\frac{-d^2}{c_2}} \quad (2)$$

$$Pulse_{width} = 1 - e^{\frac{-t_{pulse}}{250.10^{-9}}} \quad (3)$$

$$W_{coef} = e^{-0.001 Wafer_{thickness}} \quad (4)$$

$$I_{ph\_z} = (c_1 z^6 + c_2 z^5 + c_3 z^4 + c4 z^3 + c_5 z^2 + c_6 z + c_7) c_8 e^{\frac{-z^2}{20000}} \quad (5)$$

where, $d$ is the distance (in $\mu m$) between the laser spot and the center of the PN junction, $t_{pulse}$ is the laser pulse duration (in second), $Wafer_{thickness}$ is the thickness of the wafer (in $\mu m$) and $z$ is the laser lens distance (in $\mu m$) with $z = 0$ when focused on the active area. The other coefficients depend on the CMOS technology and laser lens type.

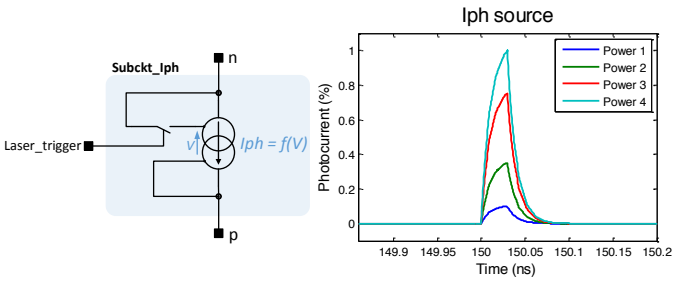


Fig. 9. Electrical modeling of a PN junction under pulsed laser stimulation

In order to simulate this photocurrent effect, the sub circuit (see Fig. 9) which contains a voltage controlled current source was built. The current amplitude of the current source is described by Eq. 1 and the start and duration of the laser pulse is set by the laser_trigger signal.

### B. *Modeling results*

Upgrading and tuning our model describes in Section V, we adjusted the parameters of the photocurrent shape for short pulses. Based on measurements with $50\,ns$ laser pulse duration, we observed that bipolar effects did not appear. Then, for the modeling, bipolar effects have been neglected and we focused only on photoelectrical effects. The sensitivity map (Fig. 10) has been extracted with low energy and a laser pulse duration of $30\,ps$. This modeling has been done with a step size of $0.1\,\mu m$ in order to be accurate in our analysis. To each point of the map, each transistors received, depending on the position and theirs sizes, a photocurrent on their active area.

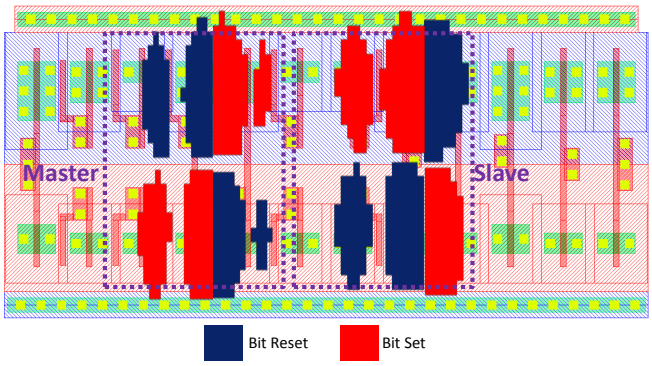


Fig. 10. Modeling results of a photoelectrical laser stimulation on a D Flip-Flop with a laser pulse duration of 30 $ps$

Fig. 10 shows the SEUs both in the master and slave latches. It corresponds perfectly with the theoretical photoelectrical sensitive junctions (Fig. 7) but presents differences compared to the experiments (Fig. 8). That can be explained because the model does not integrated the capacitors and resistivity of each transistors.

## VI. Conclusion

An analysis of the laser induced sensitive nodes of a D Flip-Flop cell was firstly reported in this paper. The preliminary conclusion of this theoretical analyze was that there are seven sensitive areas of the D Flip-Flop cell which modify the output from '0' to '1' and seven others for an output state modification from '1' to '0'. This conclusion has been verified in practice (except for only one hidden area). The topology of the cell has a strong impact on the sensitivity of a CMOS gate. The sensitive areas revealed by measurement cartographies was also confirmed by proper electrical simulations that take into account the topology of the target but without the capacitor and resistors of the nets and transistors (in a future work we will propose a model that will take account of that parameters). The validity of the approach was assessed by the good correlation obtained between electrical simulations (based on SPICE language) and measurements for this advanced CMOS technology node ($40\,nm$) which was not even analyzed both in simulation and experiments. This model could permit us to propose and to validate (on simulation basis) a new layout of a standard D Flip-Flop cell more robust against SEU. As a conclusion we can say that the electrical model presented in this paper could be an interesting tool for designer who wants to build more robust CMOS gates against SEU effects or against fault injection in the security field or to test the robustness of theirs designs.

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