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# Electrical model of an Inverter body biased structure in triple-well technology under pulsed photoelectric laser stimulation

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***Abstract*- This study is driven by the need to optimize reliability and failure analysis methodologies based on laser/silicon interactions with an integrated circuit using a triple-well process. Nowadays, Single Event Effects (SEE) evaluations due to radiation impacts are critical in fault tolerance. The prediction of a SEE on electronic device is proposed by the determination and modeling of the phenomena under pulsed laser stimulation. This paper presents measurements of the photoelectric currents induced by a pulsed-laser on an inverter in triple-well Psubstrate/DeepNwell/Pwell structure dedicated to low power body biasing techniques. It reveals the possible activation change of the parasitic bipolar transistors. Based on these experimental measurements, an electrical model is proposed that makes it possible to simulate the effects induced by photoelectric laser stimulation. Therefore this electrical model could be used as a tool of characterization for more complex CMOS circuits under Photoelectrical Laser Stimulation.**

## I. Introduction

The first faults called SEE (single event effects) have been notified in 1960s when it was found that radioactive particles were causing errors in electronic circuits [1], [2]. The aerospace industry directly affected by this issue began research on the physical effects of these particles in silicon. In this context, the use of pulsed-lasers was introduced to emulate SEEs at the experimenter's bench [3]. Nowadays, SEE is yet a major threat for semiconductor manufacturers. Photoelectric Laser Stimulation (PLS) is commonly used in reliability evaluation and failure analysis methodologies [4]. However this kind of experiments could be very expensive and time consuming. In this context, it is interesting to use a simulation tool at gate level in order to simulate with good accuracy the effect of PLS on a chip in order to analyze its impact in a very small amount of calculation time.

PLS generates electron-hole pairs in silicon, as the laser energy is greater than the silicon band gap. Our PLS experiments were carried out using a pulsed-laser at 1064 nm wavelength on the active parts of an inverter device in triple-well (designed in 90 nm STMicroelectronics CMOS technology) through their backside, a laser spot diameter of 1 µm and a laser shoot duration of 5 µs. The measurements were used to validate and calibrate the electrical model in order to create a fast and simulated SPICE solution under laser stimulation. This electrical model makes it possible to simulate the response of an inverter in a triple-well structure to laser pulses. The behavior of an inverter in triple-well under light stimulation is a good entry point to understand others more complex logic cells.

It has been shown [5], that inside the space charge region of a PN junction, electron-hole pairs will be separated by the internal electric field and then generate an optical beam induced current. The photoelectric currents created during the light stimulation flow through the PN junctions and may corrupt voltage outputs of the cells. In this paper, we also consider the parasitic bipolar junction transistors inherent to CMOS bulk devices. We show that these parasitic transistors contribute to the output cell corruption at a higher rate than just the PN junctions of the OFF MOS side. Furthermore, an electrical model of inverter biased in Psubstrate under PLS has been studied in [6]. The novelty of this paper is that our model based on actual electrical measurements takes into account the parasitic bipolar transistors topologically added by the use of a triple-well implant for the body biasing techniques (see Fig. 1).

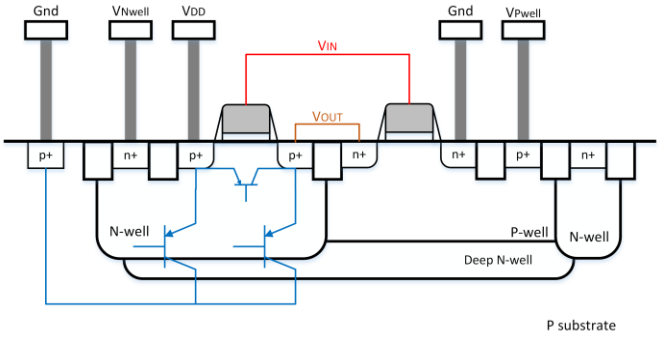



Fig. 1. Inverter DUT in triple-well technology with parasitic bipolar transistors representation

With technology scaling down, performance and power consumption play an increasingly important role in logic design. The body biasing technique presented in [7] and [8] is one well-known solution to optimize consumption and performance. This low power technique uses threshold voltage scaling by reverse or forward body bias. In 90 nm CMOS technology with

a power supply $V_{DD}$ = 1.2 V, the body biasing range is +/- 400 mV applied on both NMOS and PMOS bulks (i.e. applied on the N and P wells), where the implant DeepNwell is needed. The first electrical models of MOS transistors under pulsed laser stimulation were generally made of a current source which represents the photocurrent induced by the laser. In this paper we proposed an improvement of these electrical models in order to be capable to take into account the triple-well implant.

This article begins by explaining our models of the PN junctions under PLS as well as parasitic bipolar effects. Secondly, it shows the measurements of the inverter inside the triple-well when Input = Gnd and Input = $V_{DD}$. Finally, our electrical model and 3D simulation methods are proposed.

## II. PHOTOCURRENT ELECTRICAL MODEL

Photocurrent generated by a pulsed-laser on an IC, were generally modeled by current sources on PN junctions. We took the choice to improve the electrical model already introduced by Sarafianos et al. in [9] and [10], which takes into accounts the laser's spot size, power, pulse duration, focus of the laser beam and the spatial parameters, location, geometry, wafer thickness.

### *A. PN junction modeling*

Using the laser beams to study each junction of our structure lets us create PN junctions models (called Subckt_Iph_diode) which contain a voltage-controlled current source. The amplitude value of this current source is defined by $I_{ph}$ as expressed in (1):

$$I_{ph} = \frac{1}{\gamma}(a\,V + b)\;\alpha_{gauss}\;Pulse_{width}\;W_{coef}\;I_{ph\_z} \qquad (1)$$

where, $V$ is the reverse biased voltage, $a$ and $b$ depend on the laser power, $\gamma$ is an amplitude attenuation coefficient, $\alpha_{gauss}$ is the sum of two Gaussian functions which take into account the spatial dependency, $Pulse_{width}$ considers the laser pulse duration dependency, $W_{coef}$ is an exponential function allowing for the wafer thickness effect and $I_{ph\_z}$ is a curve function which considers the focus effect of the z axis of the laser lens:

$$\alpha_{gauss} = \beta\; e^{\left(\frac{-d^2}{c_1}\right)} + \rho\; e^{\left(\frac{-d^2}{c_2}\right)} \qquad (2)$$

$$Pulse_{width} = 1 - e^{\left(\frac{-t_{pulse}}{250\cdot 10^{-9}}\right)} \qquad (3)$$

$$W_{coef} = e^{-0.001\,Wafer_{thickness}} \qquad (4)$$

$$I_{ph\_z} = (c_1 z^6 + c_2 z^5 + c_3 z^4 + c_4 z^3 + c_5 z^2 + c_6 z + c_7) c_8\; e^{\frac{-z^2}{20000}} \qquad (5)$$

where, $d$ is the distance (in µm) between the laser spot and the center of the PN junction, $t_{pulse}$ is the laser pulse duration (in second), $Wafer_{thickness}$ is the thickness of the wafer (in µm) and $z$ is the laser lens distance (in µm) with $z = 0$ when focused on the active area. The other coefficients depend on the CMOS technology and laser lens type.

In order to simulate this photocurrent effect, the sub circuit (see figure 2) which contains a voltage controlled current source was built. The current amplitude of the current source is described by (1) and the start and duration of the laser pulse is set by the laser_trigger signal.

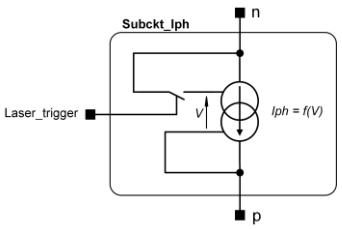



Fig. 2. Electrical modeling of a PN junction under pulsed laser embedded in a sub circuit called Subck_Iph

### *B. Parasitic bipolar transistor modeling*

We have already introduced electrical models of a triple-well structure in [11], [12] and [13], where the parasitic vertical PNP and NPN bipolar transistors were modeled as voltage-controlled current sources [14]. Parasitic bipolar transistor models can be generalized by (6):

$$I_{bip} = I_s\; exp^{\delta \frac{|V_{BE}|}{V_T}} \qquad (6)$$

where, $I_S$ is a constant used to describe the transfer characteristic of the transistor in the forward-active region (typically $10^{-14}$ to $10^{-16}$ A), $\delta$ is a modeling coefficient in order to fit the simulation and the measurements, $V_T$ is the thermal voltage and $V_{EB}$ is the voltage between N and P potentials. In order to simulate this bipolar effects, the sub circuits (see figure 3), which contains a voltage-controlled current source, were built. The current amplitude of the current source is described by (6).

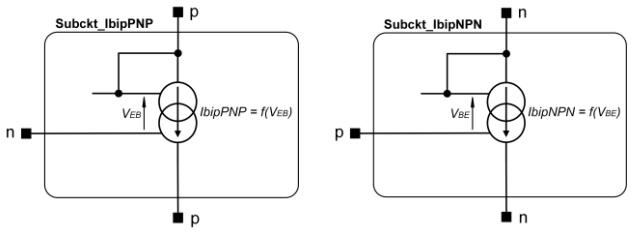



Fig. 3. Electrical modeling of the parasitic PNP and NPN bipolar transistors in a sub circuits called Subck_Ibip

## III. INVERTER MEASUREMENTS UNDER PLS

The experiments were performed with a laser spot diameter of 1 µm and a laser shoot duration of 5 µs. The Device Under Test (DUT) is an inverter inside a 70 × 70 µm triple-well stand-alone structure (see Fig. 1 for a cross-sectional view). The inverter is composed by an NMOS 630 × 90 nm and a PMOS 880 × 90 nm. The Inverter is a very basic structure but the phenomenon under PLS can be easily understood and are similar for other and more complex logical cells.

Some simulation under PLS have been presented in [6] but the novelty of this paper are the electrical measurements in order to calibrate our model of the inverter in the triple-well structure. In all the results presented, we consider that the output of the inverter holds an opposite logical state of the input. But when this inverter is stimulated by a pulse Laser, it may induce an error on the output by a logic state change. This method determines the physical effects of a SEE on the inverter in

triple-well.

First of all, it is important to well understand the different currents behavior for modeled the photocurrents generated on the PN junctions and bipolar transistors activations. From Fig. 1, we can see that three PNP bipolar junction transistors are attached to the source and drain of the PMOS transistor which may contribute to fault injection. In our measurements, the Nwell and $V_{DD}$ of our DUT were always at 1.2 V however the Psubstrate, Pwell and Gnd electrodes were grounded. The inverter is fully illuminated by the laser spot.

*A. Input = 0V*

Firstly, the input of the inverter was biased at 0 V. Then, the PMOS is used in their ON state, the NMOS in their OFF state consequently the output = 1.2 V. As shown and modeled in [12] and [13], for laser power below 50 mW, the laser induced photocurrents on the PN junctions. There are mainly 6 PN junctions (shown in green in Fig. 4) which may give rise to a photoelectric effect (DeepNwell/Psubstrate junction, DeepNwell/Pwell junction, DeepNwell/PMOS Drain junction, DeepNwell/PMOS Source junction, NMOS Drain/Pwell junction and NMOS Source/Pwell junction).

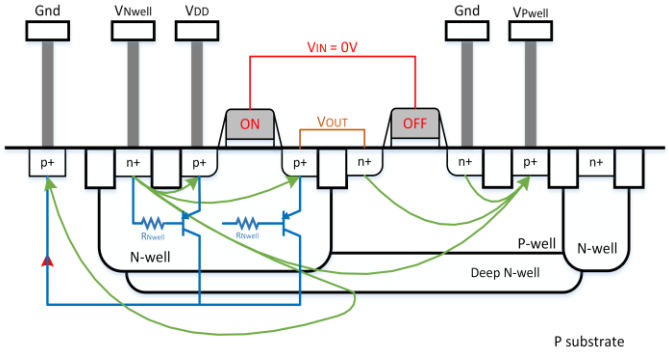



Fig. 4. Representation of the photocurrents and parasitic bipolar activations on inverter in triple-well technology when input = 0 V under PLS.

The shapes of the photocurrents measured (see Fig. 11) are similar for these interfaces but the amplitude value are widely different. Therefore the study is made independently for each PN junctions. These photoelectric effects are modeled by six sub-circuits Subckt_Iph expressed by equation (1) with different attenuation coefficients. Table I shows these coefficients for the six junctions.

Table I - ATTENUATION COEFFICIENTS MEASURED ON PHOTOELECTRIC AMPLITUDE FOR ALL PN JUNCTIONS WHEN INPUT = 0 V.

| Junction | Attenuation coefficient ($\gamma$) |
|---|---|
| *DeepNwell/Psubstrate* | 1 |
| *DeepNwell/Pwell* | 35 |
| *DeepNwell/PMOS Source* | 500 |
| *DeepNwell/PMOS Drain* | 500 |
| *NMOS Drain/Pwell* | 300 |
| *NMOS Source/Pwell* | 500 |

The main photoelectric current flows from DeepNwell to Psubstrate due to the large size of this junction. The second contributor is the DeepNwell to Pwell one, the amplitude of this photocurrent is attenuated by a coefficient 35 due to its smaller size and the Pwell doping concentration. The next contributors are significantly smaller still due to their size: the DeepNwell/PMOS Source junction, DeepNwell/PMOS Drain junction, the NMOS drain/Pwell junction and finally the NMOS Source/Pwell junction. It is well known than more the PN junction is reversed biased, more the photocurrent generated is. Consequently, the NMOS Drain/Pwell junction is more sensitive to photoelectrical stimulation than the others because it is more reversed biased (NMOS Drain = 1.2 V & Pwell = 0 V). Then its attenuation coefficient $\gamma$ = 300 is instead of 500.

It is well known that these photoelectric currents created during the light stimulation flow through the PN junctions corrupt the voltage output of the inverter. The photocurrent injected on NMOS drain/Pwell junction discharges the load capacitor and the output voltage drops. The PMOS transistor then drives current thanks to its Vds potential, which increases with the decrease of the output node. The PMOS try to maintain the output voltage high.

In addition, for laser power higher than 50 mW, a large photocurrent flows through the potential $V_{DD}$ during the laser pulse. As depicted on Fig. 5, the current on $V_{DD}$ is pulled down (negative value) as an input current direction convention.

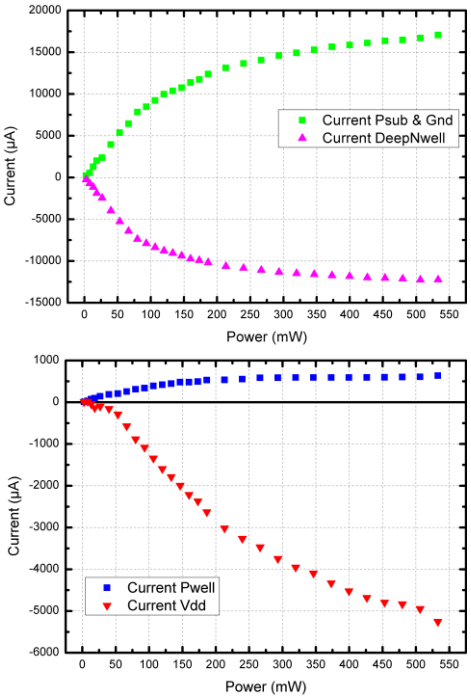



Fig. 5. Current Measurements on Gnd, DeepNwell, Pwell and $V_{DD}$ potential when Input = 0 V.

The photocurrents generated on the DeepNwell have for consequences to decrease the local DeepNwell potential. When this local potential becomes smaller than $V_{DD}$ – 0.6 V, the P+/DeepNwell junction starts conducting whereas the Psubstrate/DeepNwell junction stays reverse biased. The effect induced is the activation of the two vertical PNP parasitic

bipolar transistors P+/DeepNwell/PSubstrate (shown in blue in Fig. 4).

Furthermore, the current which flow through the Drain of the PMOS by this parasitic transistor increase the discharges of the load capacitor and the output voltage drops. This phenomenon is a second contributor to discharge the output capacitance. Finally, when the injected photocurrent is higher than the PMOS transistor saturation current, the output capacitor will be discharged and fully drop the output voltage (see in blue on Fig. 6). When the output voltage becomes smaller than $V_{DD}/2$, around 450 mW, then a fault appears. This fault is called bit-reset.

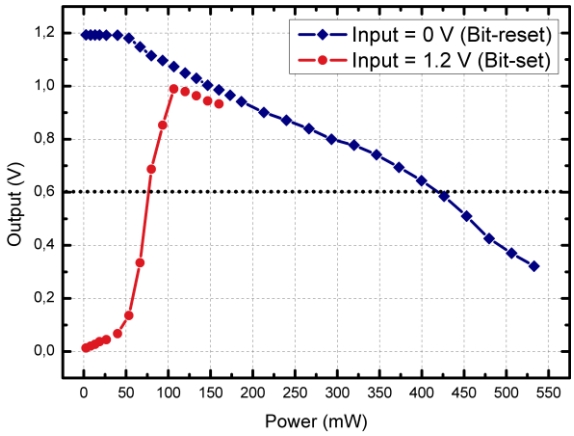



Fig. 6. Output voltage measurements on the inverter when input = 0 V & input = 1.2V.

### *B. Input = $V_{DD}$*

Secondly, the laser spot was still centered on the inverter but the input of the inverter was biased at 1.2 V. Then, the PMOS is used in their OFF state, the NMOS in their ON state consequently the output = 0 V. As previously, first the photocurrents generated on the PN junctions have been studied independently and then parasitic bipolar activations have been highlighted (see Fig. 7).

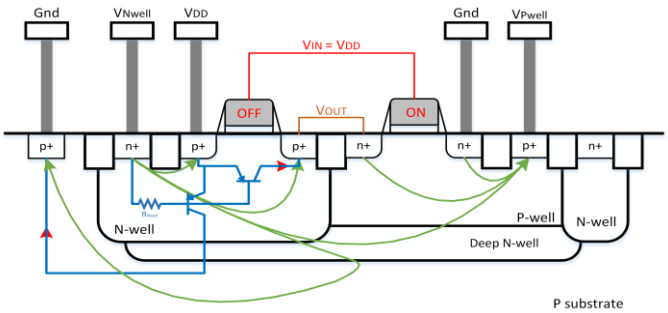



Fig. 7. Representation of the photocurrents and parasitic bipolar activations on inverter in triple-well technology when input = 1.2 V under PLS.

Table II shows these coefficients for the six junctions. For the same reason as part III.*A*, the main photoelectric current flows from DeepNwell to Psubstrate and the second one is the DeepNwell to Pwell. On the other hand, the next contributor is the DeepNwell/PMOS Drain junction due to the reverse biased condition (Nwell = 1.2 V & PMOS Drain = 0 V). The photocurrent injected on DeepNwell/PMOS drain junction has for effect to charge the load capacitor and then the output voltage rise. In this case, this is the NMOS which try to maintain the output voltage down.

Table II - ATTENUATION COEFFICIENTS MEASURED ON PHOTOELECTRIC AMPLITUDE FOR ALL PN JUNCTIONS WHEN INPUT = 1.2 V.

| Junction | Attenuation coefficient (γ) |
|---|---|
| *DeepNwell/Psubstrate* | 1 |
| *DeepNwell/Pwell* | 35 |
| *DeepNwell/PMOS Source* | 500 |
| *DeepNwell/PMOS Drain* | 300 |
| *NMOS Drain/Pwell* | 500 |
| *NMOS Source/Pwell* | 500 |

As previously noted, for laser power higher than 50 mW, a large photocurrent flows through the potential $V_{DD}$ during the laser pulse. As depicted on Fig. 8, the current on $V_{DD}$ is pulled down (negative value) as an input current direction convention. The photocurrents generated on the DeepNwell have for consequences to decrease the local DeepNwell potential and then induced the activation of one vertical PNP parasitic bipolar transistor P+/DeepNwell/PSubstrate and one lateral PNP parasitic bipolar transistor P+/DeepNwell/P+ (shown in blue in Fig. 7).

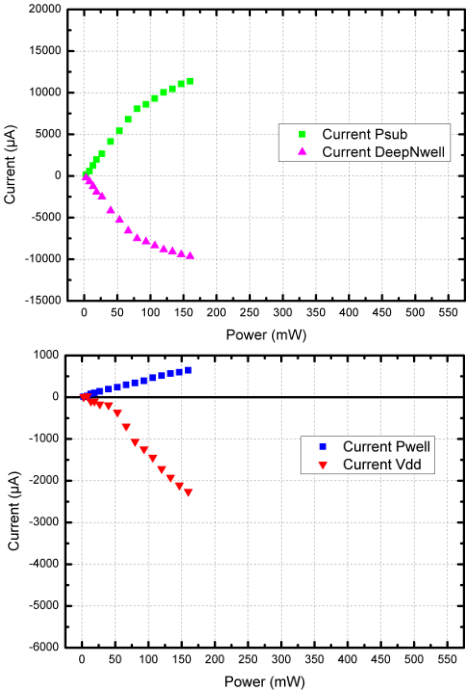



Fig. 8. Current Measurements on Gnd, DeepNwell, Pwell and $V_{DD}$ potential when Input = 1.2 V.

Furthermore, the current which flow through the Source to the Drain of the PMOS by the lateral parasitic transistor increase the charges of the output load capacitor. Then, this phenomenon is a second contributor to charge the output capacitance. This lateral bipolar (PMOS Source/DeepNwell/PMOS Drain) have

significantly more gain than a vertical one (P+/DeepNwell/PSubstrate) due to a smaller base size. The collector current generated in PMOS Drain expressed as $I_C = \beta_F I_B$ is maximized by minimizing the base bipolar width $W_B$ [6]:

$$\beta_F = \frac{1}{\frac{{W_B}^2}{2\tau_b D_n} + \frac{D_P W_B N_A}{D_n L_P N_D}} \quad (7)$$

where, $N_A$ and $N_D$ are the constants doping density in atoms/cm3 in the P-type material and N-type material, $D_N$ and $D_P$ the diffusion constant for electrons and holes, $L_P$ the diffusion length for holes in the emitter, $\tau_b$ the minority-carrier lifetime in the base.

Finally, when the injected photocurrent is higher than the NMOS transistor saturation current, the output capacitor will be charged and fully raise the output voltage (see in red on Fig. 6). When the output voltage becomes higher than $V_{DD}/2$, around 75 mW, then a fault appears. This fault is called bit-set.

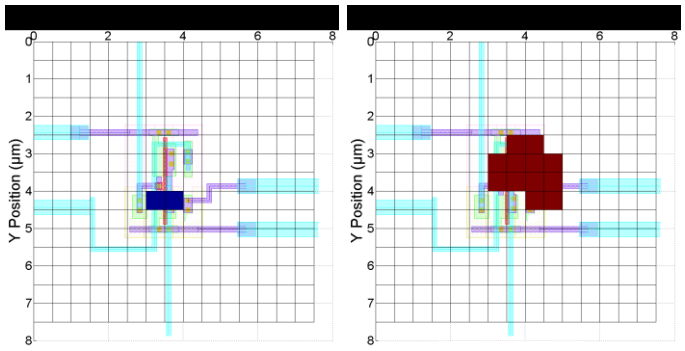
The collector current which flows from $V_{DD}$ to PMOS Drain by this lateral bipolar transistor have a significant impact on output voltage drop. From Fig. 6, we can easily notice how this parasitic PNP bipolar transistor plays an important role by drastically increased the output voltage.

The red curve (for a bit-set) stops above 170 mW because for this laser power the structure was damaged.

### *C. Sensitivity mapping measurements*

Previous theoretical work [15] (who only take into account photoelectric effects) showed that when the input = 0 V, the drain of the NMOS is 'the sensitive' part for a bit-reset and when the input = 1.2 V the drain of the PMOS is 'the sensitive' one for a bit-set. In order to validate this, experimental maps were performed. The laser power was increased progressively, until the first faults appear (for bit-set or bit-reset).

The SEE sensitivity mapping (8 µm x 8 µm with a step size of 0.5 µm) we have obtained is drawn in Fig. 9. Blue color is used to depict a bit-reset at laser power = 426.4 mW and the red for a bit-set at laser power = 93.275 mW. The two cartographies are for different laser powers due to the difference sensitivity of a fault between the two failure modes.




(a) Bit-reset (b) Bit-set

Fig. 9. SEE sensitivity measurements maps of the inverter in triple-well for a bit-reset at laser power = 426.4 mW (a) and a bit-set at laser power = 93.275 mW (b).

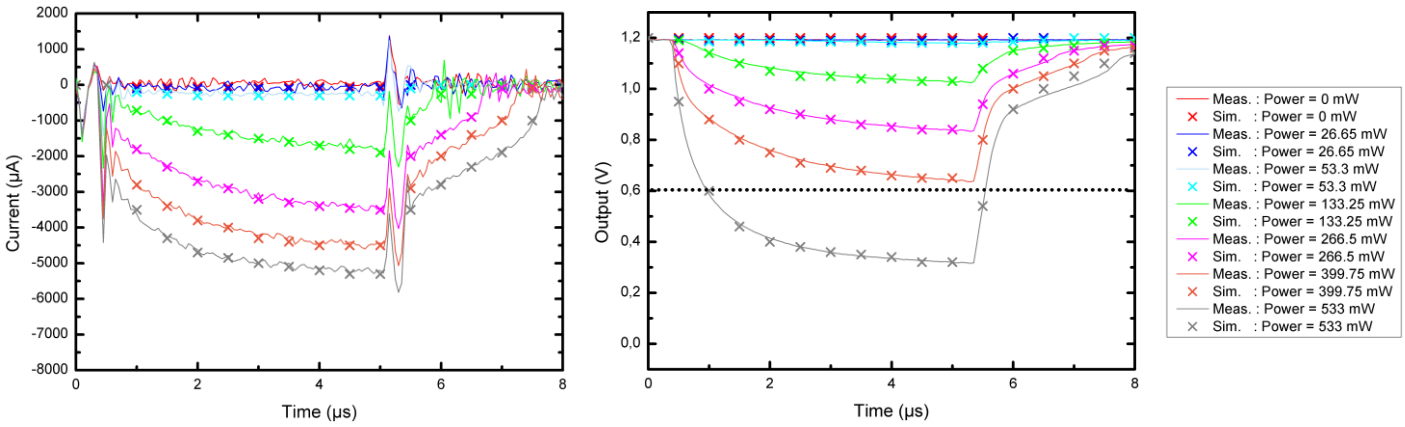
The two maps revealed that: NMOS Drain is the sensitive area for a bit-reset; on the other hand, all the Nwell area is sensitive for the bit-set. This is due to the photocurrent generated on Nwell which induce the activation of parasitic bipolar.

## IV. ELECTRICAL MODELING OF THE INVERTER UNDER PLS

In this section we present post-layout SPICE simulation of our DUT with the various photoelectric and parasitical bipolar transistors model effects we built. The aim of this modeling is to validate our methodology in order to explore some specific results with a very fast calculation time.

### *A. Model and electrical simulation*

For every PN junction and parasitic bipolar transistor, a sub circuit which contains a specific controlled voltage current source (presented in part II) is added to the netlist. These models were validated and tuned thanks to electrical measurements (presented in part III), in order to take into account laser condition and body biasing variations.




(a) Current on $V_{DD}$ (b) Output potential

Fig. 11. Comparison of experimental and simulation results of the current on $V_{DD}$ (a) and output potential (b) of an inverter in triple-well under PLS when input = 0 V.

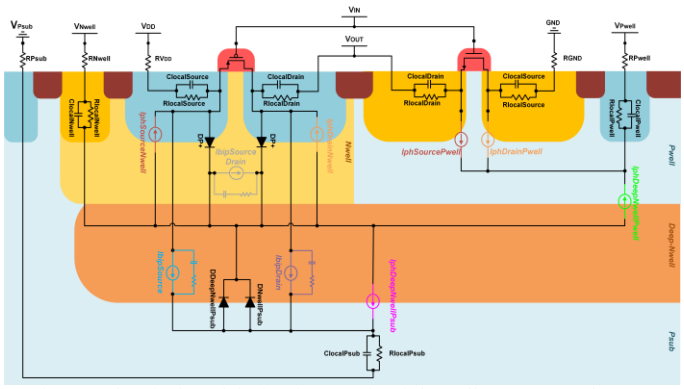


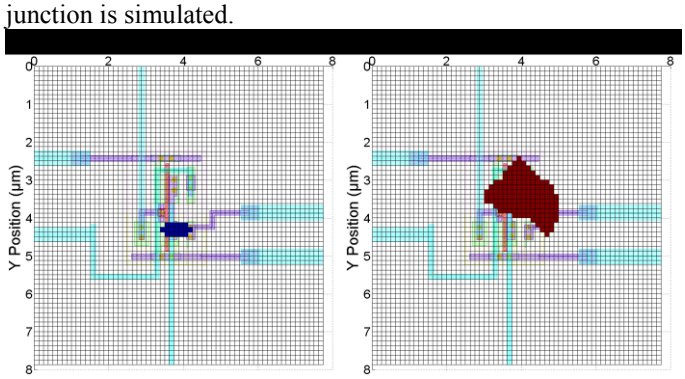

Fig. 10. Electrical model of an inverter in triple-well structure under PLS.

Photocurrents have been simulated with our model on the PMOS, NMOS and different wells of our DUT. Fig. 11 presents the current on VDD and the output potential. A very good correlation is obtained between simulation and measurements.

*B. Sensitivity mapping simulation*

Moreover, our model takes into account the spatial parameters, making it possible to draw current cartographies.

Firstly it is necessary to create a meshing (in our case, a step equal to 0.125 µm) on the layout of the cell. For each point of the mesh, the distance between this point and all the PN junction centers are measured. Mainly thanks to Equation (2), for each point of the mesh, the photocurrent generated by every PN junction is simulated.




(a) Bit-reset (b) Bit-set

Fig. 12. SEE sensitivity simulation maps of the inverter in triple-well for a bit-reset at laser power = 426.4 mW (a) and a bit-set at laser power = 93.275 mW (b).

Sensitivity maps obtained from simulations (Fig. 12) and measurements (Fig. 9) showed a very good correlation. This confirms the good results already obtained on single test transistors [11], [12], [13] and validates the relevance of our simulation tool for more complex logic gates.

## V. CONCLUSION

This paper describes an accurate electrical model of an inverter in triple-well in 90 nm CMOS technology that takes into account parasitic bipolar activations under pulsed-laser stimulation. This model combines all various photoelectrical phenomenon revealed by measurements during the PLS. The effectiveness of our approach has demonstrated a very good correlation between measurements and our model. In failure analysis, this proposed simulation technique may serve as a reference to detect defaults by comparison with a device under pulsed-laser stimulation. Future works will consist in characterizing and modeling complex logic gates inside a triple-well process.

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