Influence of triple-well technology on laser fault injection and laser sensor efficiency

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Influence of triple-well technology on laser fault injection and laser sensor efficiency

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***Abstract*— This study is driven by the need to understand the influence of a Deep-Nwell implant on the sensitivity of integrated circuits to laser-induced fault injections. CMOS technologies can be either dual-well or triple-well. Triple-well technology has several advantages compared to dual-well technology in terms of electrical performances. Single-event responses have been widely studied in dual-well whereas SEE (single event effects) in triple-well is not well understood. This paper presents a comparative analysis of soft error rate and countermeasures sensors with for these two techniques in 40 nm and 90 nm CMOS technology. First, laser fault injection on registers were investigated, showing that triple-well technology is more vulnerable. Similarly, we studied the efficiency of Bulk Built-In Current Sensors (BBICS) in detecting laser induced fault injection attempts for both techniques. This sensor was found less effective in triple-well. Finally, a new BBICS compliant with body-biasing adjustments is proposed in order to improve its detection efficiency.**

***Index Terms*— Laser, fault injection, triple-well, body biasing, countermeasure**

I. INTRODUCTION

The first faults called SEEs have been notified in the 1960s when it was found that radioactive particles were causing errors in electronic circuits [1], [2]. The aerospace industry directly affected by this issue began research on the physical effects of these particles in silicon. In this context, the use of pulsed-lasers was introduced to emulate SEEs at the experimenter's bench [3]. Laser-fault injection and radiative particles have indeed similar effects on system on chip. However, pulsed-laser may also be used to induced faults (as a result of SEEs) into the computations of security-dedicated ICs for the purpose of retrieving the secret data they may contain [4], [5]. BBICS [6] were introduced to monitor the unusual currents induced in the bulk of integrated circuits (ICs) by ionizing particle hits.

A. Laser-induced Single Event Effects in Integrated Circuits

When an ionic particle or a laser beam passes through silicon it generates electron-hole pairs along its path. These electrical charges generally recombine without any significant effect on the IC computations. However the electric field found in reverse-biased PN junctions may separate the electron-hole pairs, inducing a parasitic transient current. This transient current may in turn disturb the voltage of the IC's internal nodes leading to computational errors. This pulsed laser phenomenon may appear provided that its photons energy is bigger than the silicon bandgap (electron-hole pairs are then induced by photoelectric effect [7]). This effect is called 'photocurrent' [8]. The way how a transient photocurrent is turned into a SEE is illustrated in Fig. 1 for the inverter case when its input is at low logical level.

In this configuration, the SEE sensitive area is the drain of the NMOS transistor (shaded in pink), which is in OFF state. A laser-induced photocurrent, depicted by a current source in Fig. 1, may be injected there through the reverse-biased PN junction between the N-type drain of the NMOS (biased at VDD) and the P-type substrate (grounded). As a result of the latter, the inverter output voltage may drop from '1' to '0' provided that the injected photocurrent is higher than the PMOS transistor saturation current. Note that a similar phenomenon may also take place when the inverter input is at a high logical state (in this instance the laser-sensitive place is the drain of the OFF PMOS): the photocurrent then flows from VDD through the biasing contact (or tap) of the Nwell (i.e. the PMOS bulk) to ground. This voltage transient, also known as SET (Single Event Transient), may thus propagate through the circuit logic, creating errors. Furthermore, if a SET is induced directly in a memory element, as a latch, the stored data may be flipped, characterizing the so-called SEU (Single Event Upset; i.e. a bit set from '0' to '1' or a bit reset from '1' to '0').

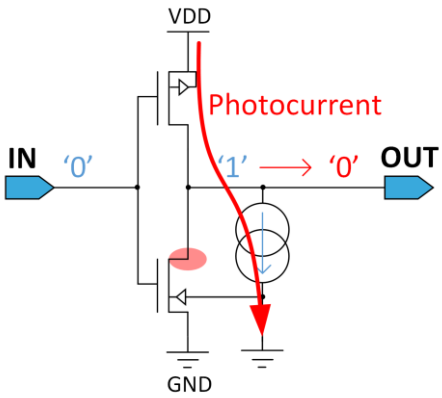
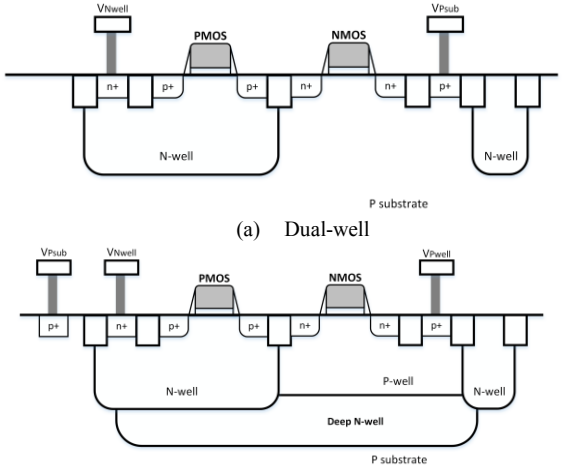


Figure 1. Laser-sensitive area of an inverter with its input at low level.

B. *Triple-well isolation*

The use of a triple-well layer is used to electrically isolate the Pwell in order to reduce the electronic noise and cross talk from the substrate. It may also be used to adjust power consumption and speed of the transistors by modifying the threshold voltage using well bias. Typically, devices are regularly distributed along cell array in dual-well (also called in bulk technology): Nwell and Psubstrate rows (Fig. 2a). In triple-well, a Deep-Nwell implant (DeepNwell) is used to isolate the substrate of the NMOS transistors from the Psubstrate of the chip, hence creating Pwells. The biasing of the DeepNwell at VDD (generally) is provided through the Nwell. Such as, Psubstrate potential and Pwell may be at different voltage potential (but generally grounded). In triple-well, cells are places in Nwell and Pwell array (Fig. 2b).



(a) Dual-well

(b) Triple-well

Figure 2. Cross section view of CMOS gates (a) without triple-well and (b) with triple-well.

Since the first SEEs, semiconductor industry searches to improve architecture and process technology against soft error. The use of triple-well has been widely studied against SER in radiation evaluation. In 1984, Momose *et al.* [9] showed that the use of a Deep P-type implant in an N substrate of a RAM memory is an excellent protection against SEE. It decreases the soft error rate (SER) susceptibility by a factor of 10^{+03}. Then between 1985 and 1993, similar studies [10] and with Deep N-type implant in a P substrate [11] and [12] also showed significant reduction factors of SER between 100 and 10^{+03}. Afterward, studies of more recent technology nodes showed less conclusive results. [13] and [14] found gains of 40% on 0.18µm and 0.15µm for SRAM with triple-well. Then [15], [16], [17] proved that the more technologies become thin (180 nm, 130 nm, 90 nm, 65 nm and 40 nm), the more the SER becomes important. And [18] shows that the triple-well may even have a negative impact on SER.

This paper is organized as follows: Section II describes comparative experiments of laser fault injection in dual-well and triple-well technology in 40 nm technologies. In section III, the principles underlying BBICS and its architecture are described. A comparison for both in dual-well and triple-well has been experimentally drawn. Its weaknesses on the basis of measurements, revealed during the testing, are discussed. In section IV, we propose BBICS architectural modification to obtain an improved detection capability. A new design well suited for triple-well CMOS is introduced. Then, section V draws a conclusion

II. FAULT INJECTIONS COMPARISON

Fault injection were performed with a pulsed-laser at 1064 nm wavelength, a laser spot diameter of 1 µm and a wide range of laser pulse duration from short nanosecond to long microsecond. The laser beam was centered on flip-flops in dual-well and triple-well structures through their backside. Our test structures were designed in 40 nm CMOS STMicroelectronics technology for both techniques (dual and triple-well). The targeted flip-flop design and layout were similar. All the datas in this paper were normalized with a single percentage factor (instead of power in watts) for effective presentation and due to confidentiality constraints. These laser settings are not consistent with the emulation of an ionizing particle strike. However, we were more interested in comparing the magnitude of laser power needed for a fault injection than in precisely emulating an SEE.

Multiples faults were recorded during the experiments on the test structures. In figure 3 are compared the minimum laser power needed for a fault injection on the structure with and without triple-well.

These data show that the minimum laser power needed for an SEE on a FF in triple-well are around 2 times lower than in dual-well. This trend and order of magnitude for the slight decrease are in agreement with the other works published in the literature [18]. Nowadays, for a 40 nm CMOS technology, the use of a triple-well has a negative impact regarding SEE generation with a laser.

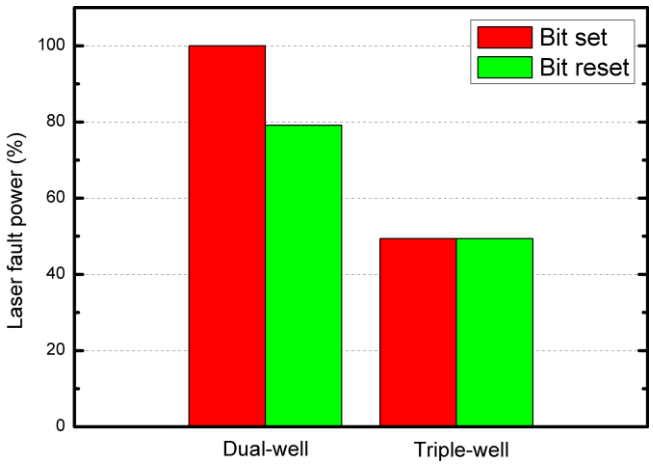


Figure 3. Comparative study of the laser sensitivity threshold of a flip-flop in dual-well and triple-well.

III. SENSOR BBICS COMPARISON

A fecund idea of countermeasure was the monitoring of the currents that happen with SEEs [19], [20]. Bulk Built-In Current Sensors (BBICS) were developed to detect the

transient bulk currents induced in the bulk of integrated circuits when hit by ionizing particles or pulsed laser [6], [21], [22]. Among various BBICS architecture proposals, only few were, to date, experimentally tested [22], [23]. A simulation-based evaluation of a BBICS used to monitor a triple-well architecture was done by [26]. Their conclusion was to recommend the use of triple-well to obtain an optimal use of BBICS.

Our experimental evaluations are dedicated to compare and validate the efficiency of the sensor of a BBICS architecture, designed to simultaneously monitor PMOS and NMOS transistors in dual-well and triple-well structures, under Photoelectric Laser Stimulation (PLS). The obtained results are the first silicon experimental proof of the efficiency of BBICS in triple-well and the mitigated results compared with the dual-well BBICS. Furthermore our investigations will give spatial information of the sensitivity detection.

A. BBICS principles

Bulk currents induced during normal operation of an IC are in the µA range, whereas particles or laser-pulsed induce bulk currents are above by two orders of magnitude for the generation of SEEs [6]. BBICSs are designed to take advantage of this property: they monitor bulk currents, hence they are able to detect unusual currents and, consequently, the advent of SEEs [24], [25].

Fig. 4 depicts the insertion of BBICS between the bulks of the MOS transistors and their biasing voltages. The BBICS used pBBICS to monitor PMOS bulk transistors (i.e. the Nwell), and nBBICS to monitor NMOS bulk transistors (i.e. the Psubstrate in dual-well and the Pwell in triple-well structure).

Hence, as illustrated, any transient photocurrent necessarily flows through the BBICS. The purpose of the BBICS is then to raise a warning flag indicating that the circuit function may be affected. Note that the BBICS has also to provide the

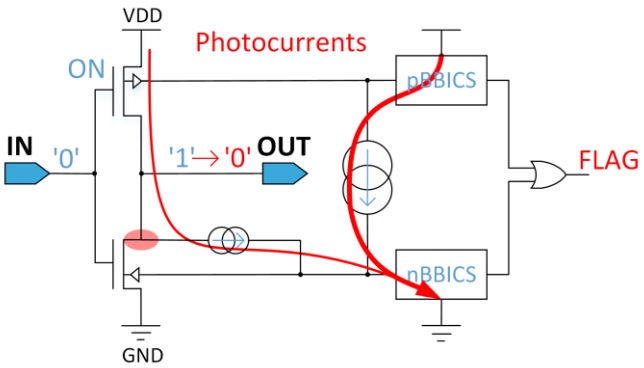


Figure 4. Principle of SEE detection by a combinated n & p BBICS

biasing of the transistor's bulk.

B. BBICS architecture

Fig. 5 depicts the architecture of the BBICS we designed and used for practical validation with a laser in [23]. Its main feature is its ability to simultaneously monitor NMOS and PMOS transistors. Two cross-coupled inverters are used to store the content of a warning flag: OUT node. OUT goes to high level to indicate the detection of any unusual bulk current, and stays low in monitoring mode. The INNWELL and INPWELL nodes are the respective BBICS connections to the biasing contacts of the PMOS and NMOS bulks. Transistors MP1 and MN1 are used to bias the INNWELL and INPWELL nodes, respectively at VDD and ground. In this way they ensure the proper biasing of the corresponding bulks. These transistors are always in ON state. The purpose of transistors MP2 and MN2, whose drains are connected to nodes OUTB and OUTA, is to raise the alarm flag in case of the advent of a SEE according to the process explained hereafter. Fig. 5 also highlights (in violet) when a bulk current is induced by the laser, OUTA and OUTB change their stable state in the latch, so consequently, the output of the sensor (OUT) is at '1'. The sensitive latch detects small variations of their inputs and memorizes a state if there was a transient bulk current. It needs to be reset at every acquisition.

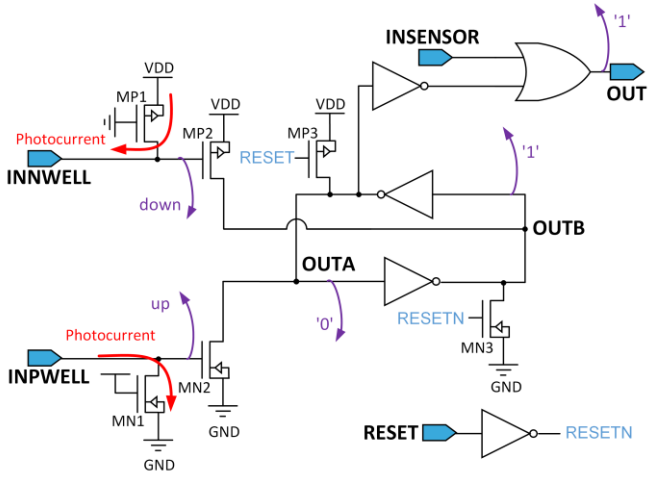


Figure 5. BBICS architecture and principle of SEE detection

C. Experimental measurements

For the purpose of analyzing the weakness of the BBICS, we performed a set of experiments on a test chip we designed in 90nm CMOS STMicroelectronics technology. Note that the technology node differs from the fault injection evaluation presented in part II. But the tendency stays the same in 40 nm (simulation have been done in the next part). Manufacturing silicon BBICSs in 40 nm are in progress. Sensor detection measurements will be evaluated soon.

Our test structure in 90 nm, is the same as used for our results presented in [23]. We focused our study on two same areas of a purely combinational logic block, in dual-well and triple-well technologies, monitored by a single BBICS. These measurements were carried out by the same infrared laser source used in section II, for a laser power = 100% (minimum power fault threshold in dual-well) and for a wide range of laser pulse duration from short ns to long µs.

To understand the different detection maps reported in Fig. 6, description of how the blocks are distributed in the layout is

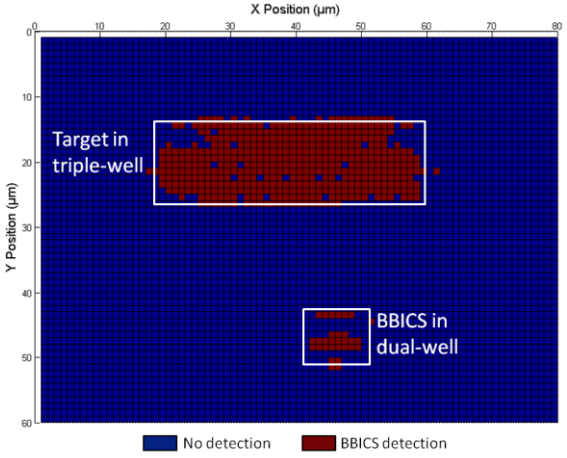
important. The 45 µm x 13 µm monitored area (also called target) is 14 µm far from the BBICS in order to avoid any perturbation during acquisitions. This target is a combinatorial gates area whose bulks are biased by the BBICS. Two version of this gates area have been designed in dual-well and triple-well technologies in order to have a comparative sensitive detection area. The BBICS, is always designed in dual-well. The laser detection maps will cover both the monitored area and the BBICS (80 µm x 60 µm with a step size of 1 µm).

A first detection (or sensitivity) maps at 100% laser power, is shown on Fig. 6a. The target sensitive area is almost fully covered in triple-well. Our measurements were caring out, first in triple-well in order to have the laser power needed to have a full coverage. Firstly, it is the proof of the effectiveness of a laser sensor in triple-well technology. Unfortunately, for this coverage, the laser power is 2 times higher than the power requested for a SEE in a flip-flop (cf part II).

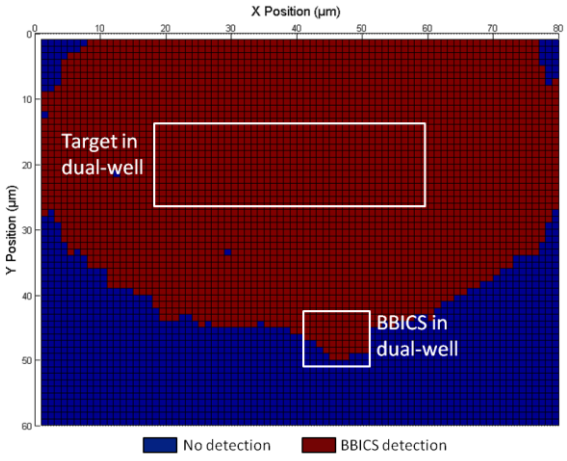
Then, a second detection maps in dual-well (Fig. 6b) was built experimentally to have a comparative detection trend from the previous detection maps. The sensitive area in dual well is 6.4 times bigger than in triple-well. This result is contradictory with [26]. Our hypothesis is that the current generated on the wells in triple-well are less important than in dual-well.

A detection area is also present in the BBICS itself. It is not due to the photocurrent in the BBICS taps but to an SEU in the core latch of the BBICS itself.

The architecture of this single BBICS demonstrated that the detection is very effective in dual-well technology but not enough in triple-well. So the design need to consider those aspects to perfectly tune the BBICS detection threshold. It can be tuned by changing the W/L ratio of MN1 and MP1 transistors. The more resistive these transistors are, the more effective the detection at low photocurrent is. Unfortunately, after the design the sensor coverage can't be adjusted.



(a) Triple-well



(b) Dual-well

Figure 6. BBICS laser cartographies in (a) triple-well and (b) dual-well, for a laser power = 100%.

IV. THE USE OF BODY-BIASING FOR THE SENSOR

Based on these results, we developed a new BBICS architecture well suited for the monitoring of triple-well CMOS logic and with the goal to adjust the BBICS coverage.

With technology scaling down, performance and power consumption play an increasingly important role in logic design. The body biasing technique presented in [27] and [28] is one well-known solution to adjust consumption and performance. This low power technique uses threshold voltage scaling by reverse or forward body bias. In 40 nm CMOS technology, the power supply is 1.2 V and the body biasing range is +/- 400 mV applied on both NMOS and PMOS bulks (i.e. applied on the N and P wells). Body-biasing technique can only be obviously used for the triple-well CMOS. The Psubstrate potential is always grounded, DeepNwell = 0.8 V and Pwell = 0.4 V in the maximal Forward Body Biasing (FBB) condition and DeepNwell = 1.6 V and Pwell = -0.4 V in the maximal Reverse Body Biasing (RBB) condition. The aim of the present work is to use the influence of FBB and RBB conditions on the BBICS sensitivity coverage.

As we explained on part III.B, when a laser induces photocurrent, it flows through MP1 & MN1, and then charges

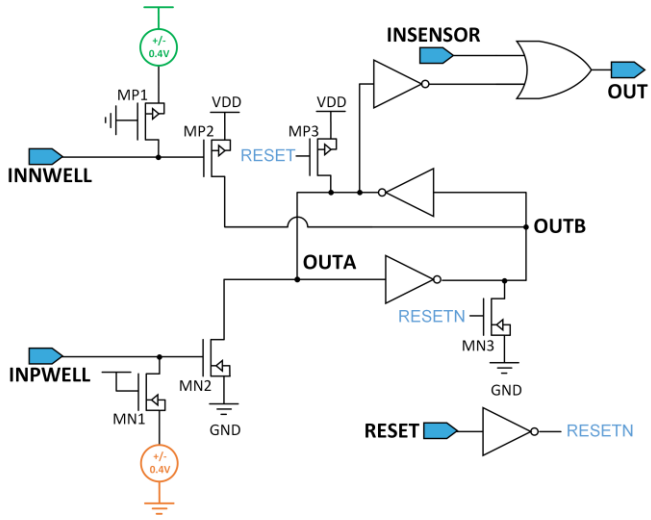


Figure 7. BBICS architecture compliant with body-biasing variation.

or discharges the gates capacitances of transistors MP2 and MN2. As a result, node INPWELL (NMOS bulk's voltage) rises and INNWELL (PMOS bulk's voltage) falls, hence MP2 and MN2 pass from OFF to ON state making the core latch flip. Then, in FBB condition the INPWELL potential is intentionally scaling up and the INNWELL potential scaling down. This biasing tuning will have the impact to help the BBICS detection. Thus, in RBB condition the potential are inversed and then the impact will disadvantage the BBICS detection. Based on this assumption, we designed a BBICS compliant with body-biasing adjustments (see Fig. 7). MP1 and MN1 ensure the proper biasing of the corresponding bulk. Then, the source potential instead of being directly connected to VDD and GND, they are connected on adjustable voltage source in green and orange on Fig.7.

For the purpose of analyzing the BBICS coverage, we performed a set of experiments on stand-alone structures to measure the currents involved in SEE generation. These measurements were carried out on NMOS and PMOS transistors for both dual-well and triple-well [29], [30] and [31]. Based on these measurements, we created SPICE simulation models which make it possible to simulate the photocurrent generated on the test structure. Fig. 8 reports the signals of interest during a laser shot: the transient currents generated on Nwell, the voltage of INPWELL (NMOS bulk's voltage) and INNWELL (PMOS bulk's voltage) and the flag signal OUT.

The next step was to obtain the detection threshold (i.e. the transient current magnitude sufficient to trigger an alarm) of the new BBICS with body-biasing well adjustments. The transient current magnitude was progressively increased (the pulse timings were left unchanged) until reaching the magnitude sufficient to trigger the alarm. We ran simulations for different FBB & RBB variations. The obtained results are given in table 1.

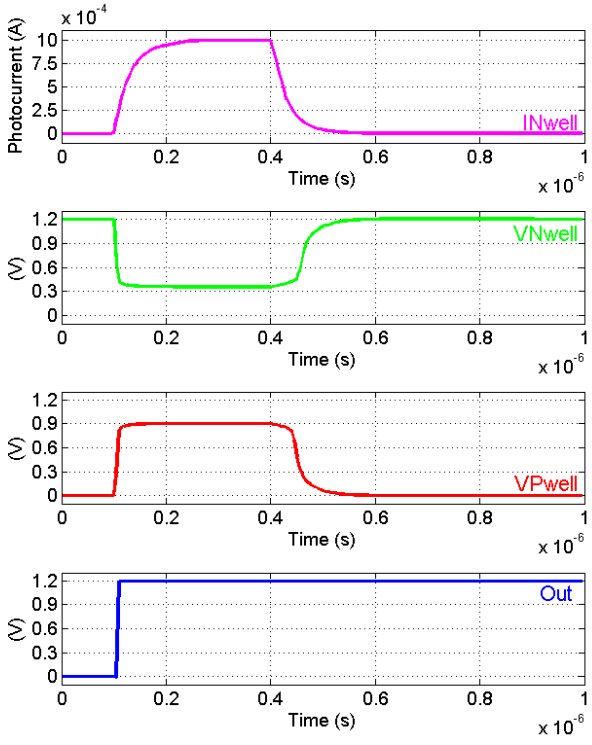


Figure 8. Electrical BBICS simulation whithout body-biasing.

TABLE I. EFFECT OF BODY-BIASING ON BBICS DETECTION THRESHOLD

Body-biasing	DeepNwell potential (V)	Pwell potential (V)	DeepNwell Current (µA)	Pwell current (µA)	Laser power (%)
RBB	1.6	-0.4	309	204	199.74
	1.4	-0.2	231.5	152.8	149.64
No	1.2	0	154.7	102.1	100
FBB	1	0.2	82.9	54.7	53.59
	0.8	0.4	23.7	15.64	15.32

The first three columns show the body-biasing condition and the voltage potential of the Nwell and Pwell. The fourth and fifth columns are some currents extract values of the photocurrent generated on the wells. The photocurrent generated on Nwell is around 50% higher than in Pwell. This is because one part of this current flows to Psubstrate. And this current is not monitored by the BBICS structures. And the last column is the minimum laser power needed for BBICS detection (also called detection threshold).

As we expected, the FBB condition contributes to help BBICS detection and the RBB condition limits this impact. In FBB condition, the Pwell/DeepNwell junction is less reversed biased (0.8 – 0.4 = 0.4 V) than in RBB condition (1.6 + 0.4 = 2 V). It is well known that the more the PN junction is reverse biased, the more the photocurrent is generated. Thus, in RBB condition the photocurrent on DeepNwell is 309 µA and only 23.7 µA in FBB. This current generation should be limiting the BBICS detection in FBB. However, the threshold voltage V_{th} of the transistor MP2 and MN2, decrease in FBB condition than in RBB. In addition, FBB changes the gate potential of MP2 and MN2. Then, it drastically helps the sensor detection by reaching the voltage gates of MP2 and MN2 to the ON state.

Therefore, in maximal FBB condition, the minimal laser power needed for a BBICS detection is 15.32%. Compare to, the previous results, this laser power is now too weak to induce a SEE in flip-flops. Thus, the use of FBB on BBICS compliant with body-biasing in triple-well structure appears to solve the weakness for detecting a SEE.

V. CONCLUSION

This paper compares the triple-well structure to a classical dual-well. Test results for laser fault injection show that triple-well flip-flops cells are more vulnerable compared to dual-well. Additionally, triple-well BBICS countermeasures are less sensitive than in dual-well. Our experiments revealed an unexpected weakness in using triple-well contrary to the work simulated by [26]. Then, we proposed a new BBICS compliant with body-biasing adjustments. This solution shows the effective impact on detection and can easily used as an

adjustment of the sensor threshold, in order to improve its detection efficiency.

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