



HAL
open science

Laser testing of a double-access BBICS architecture with improved SEE detection capabilities

Clément Champeix, Jean-Max Dutertre, Vincent Pouget, Bruno Robisson,
Mathieu Lisart, Nicolas Borrel, Alexandre Sarafianos

► **To cite this version:**

Clément Champeix, Jean-Max Dutertre, Vincent Pouget, Bruno Robisson, Mathieu Lisart, et al..
Laser testing of a double-access BBICS architecture with improved SEE detection capabilities. 2016
16th European Conference on Radiation and its Effects on Components and Systems (RADECS), Sep
2016, Bremen, Germany. 10.1109/RADECS.2016.8093172 . emse-01855833

HAL Id: emse-01855833

<https://hal-emse.ccsd.cnrs.fr/emse-01855833>

Submitted on 8 Aug 2018

HAL is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers.

L'archive ouverte pluridisciplinaire **HAL**, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.

Laser testing of a double-access BBICS architecture with improved SEE detection capabilities

Clément Champeix^{*†}, Jean-Max Dutertre[†], Vincent Pouget[§], Bruno Robisson[‡], Mathieu Lisart^{*},
Nicolas Borrel^{*} and Alexandre Sarafianos^{*}

^{*}STMicroelectronics, Secure Microcontrollers Division (SMD), Rousset, France

[†]Ecole Nationale Supérieure des Mines de Saint-Etienne, Secure Architectures and Systems (SAS)
Centre de Microélectronique de Provence, Gardanne, France

[‡]CEA-TECH, Gardanne, France

[§]IES, Montpellier, France

clement.champeix@emse.fr | clement.champeix@st.com | +33442688195

Abstract—The paper reports the experimental validation of a new Bulk Built-In Current Sensor (BBICS) designed and implemented in a 40nm CMOS technology. The double-access architecture provides improved SEE detection as confirmed by laser experiments.

Keywords—Bulk Built-In Current Sensor, Radiation-hardening by design, Single-Event Effects, Laser fault injection, SEE detection

I. INTRODUCTION

When exposed to an harsh environment in space, high atmosphere or even on earth, integrated circuits (ICs) may undergo soft errors. Among the various existing effects, Single-Event Effects (SEEs) due to ionizing particles may result in a faulty behavior of the circuit. Many radiation hardening by design (RHBD) techniques have been proposed in order to deal with SEE at cell or circuit level. Those techniques rely on various strategies including critical charge increase, critical node redundancy, event detection and correction. A fruitful idea was the monitoring of the currents that happen with SEEs [1]. This idea found its development in the principle of Bulk Built-In Current Sensors (BBICS) which were developed to detect the transient current induced in the bulk of ICs when hit by ionizing particles [2], [3]. BBICS are particularly well suited at detecting dynamic errors associated to single-event transients (SET) that can not be detected by more classical static error detection and correction (EDAC) architectures.

This paper introduces the architecture of the double-access BBICS we developed. This BBICS architecture was embedded in a 40nm CMOS test chip. Its ability at detecting SEEs was tested with a picosecond range laser source. These experiments revealed its high efficiency: the BBICS detection threshold was found lower than the SEE occurrence threshold.

II. BBICS PRINCIPLES

Bulk currents induced during normal operation of an IC are typically in the μA range; whereas particle-induced bulk currents have to be above two orders of magnitude to generate an SET on the related gate output [2]. BBICSs are designed to take advantage of this property: they monitor bulk currents

(i.e. currents passing through P-taps and N-taps), hence they are able to detect unusual radiation-induced currents and, consequently, the appearance of SEEs [4], [5].

Fig. 1 depicts the insertion of a BBICS between the bulk (i.e. the Psubstrate) of NMOS transistors and the ground. Hence, as illustrated, any SEE transient current necessarily flows through the BBICS. The purpose of a BBICS is then to raise a warning flag indicating that the circuit function may be affected. Note that the BBICS has also to provide the biasing of the transistor's bulk, a ground biasing in case of NMOS. In Fig. 1, the BBICS used to monitor NMOS transistors is named nBBICS. There also exists pBBICS dedicated to the monitoring of PMOS transistors.

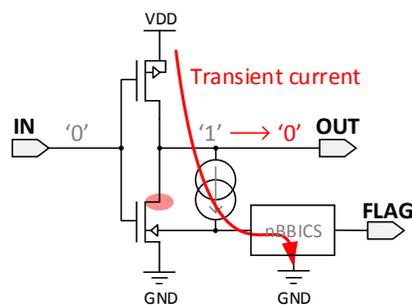


Fig. 1. Principle of SEE detection by an NMOS dedicated nBBICS

III. ARCHITECTURE OF THE DOUBLE-ACCESS BBICS USED IN THE EXPERIMENTS

A. Double-access BBICS architecture

Fig. 2 depicts the architecture of the BBICS we designed and used for practical validation. Its main feature is its ability to simultaneously monitor NMOS and PMOS transistors. Two cross-coupled inverters are used to store the content of a warning flag: OUT node. OUT goes to high level to indicate the detection of any unusual bulk current, and stays low in monitoring mode. The INNWELL and INPWELL nodes are the respective BBICS connections to the biasing contacts of the PMOS and NMOS bulks. Transistors MP1 and MN1 are used

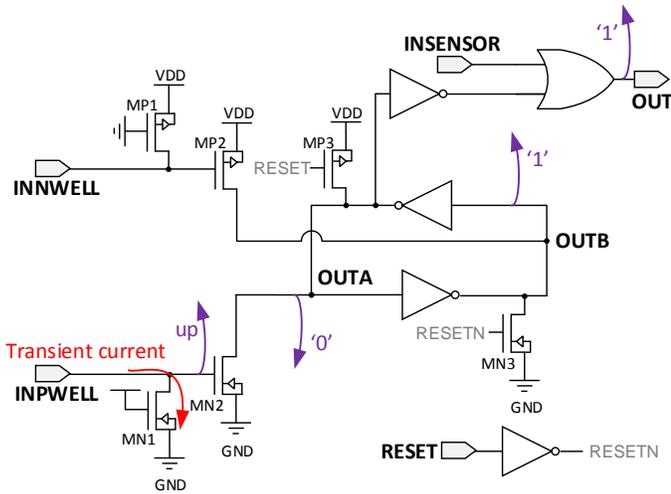


Fig. 2. Double-access BBICS architecture and principle of SEE detection

to bias the INNWELL and INPWELL nodes, respectively, at VDD and ground. In this way they ensure the proper biasing of the corresponding bulks. These transistors are always in ON state. The purpose of transistor MP2 and MN2, whose drains are connected to the OUTB and OUTA nodes, is to raise the alarm flag if an SEE is detected according to the process explained below. The double-access BBICS architecture also has a reset mechanism (RESET input) thanks to transistors MP3 and MN3. Finally an inverter and an OR2 gate inserted between OUTA and OUTB nodes make it possible to aggregate several alarm flags into a single one by using the INSENSOR input.

Fig. 2 also highlights (in violet) the chain of events involved in bulk current detection by the BBICS when a transient current flow through P-taps.

When a bulk current is induced by an ionizing particles, OUTA and OUTB change their stable state in the latch, so consequently, the output of the sensor (OUT) is at '1'. The latch should be very sensitive to detect small variations of their input voltage. The latch memorizes a state if there was a transient bulk current, so it needs to be reset at every acquisition.

B. Simulations

Electrical simulations may be done to determine the ability of BBICS at detecting SEEs, with an ideal current source, modeling transient current induced by SEE [6]. Current amplitudes and pulse durations (respectively from $1 \mu A$ to $300 \mu A$ and from $5 ps$ to $320 ps$) were simulated in order to determine the detection sensitivity. Two circuits are evaluated: a nBBICS (which architecture was derived from that of Fig. 2 by removing transistors MP1 and MP2) and a double-access BBICS to validate the usage of the second circuit.

Fig. 3 depicts the transient voltages inside the sensor with a comparison between a nBBICS and a double-access BBICS for the same transient current parameters ($200 ps$ and $12 \mu A$) emulating a SEE. The nBBICS failed at detecting the event whereas the double-access BBICS succeeded thanks to the toggle of latch on the both sides.

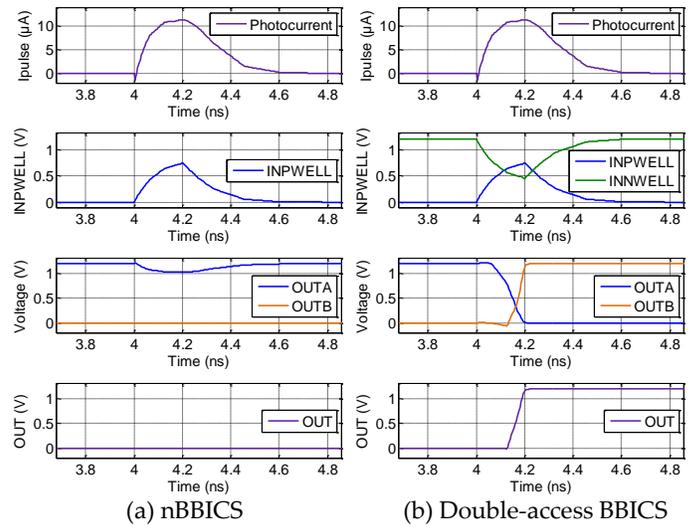


Fig. 3. Simulation results of nBBICS and double-access BBICS detecting transient currents ($200 ps$ and $12 \mu A$)

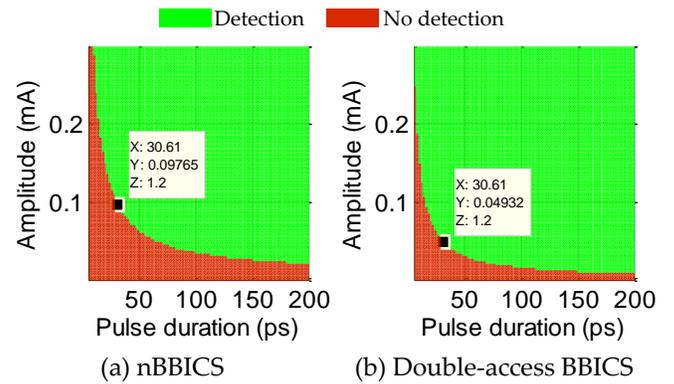


Fig. 4. SEE detection behaviors of the nBBICS and double-access BBICS as a function of the current pulse amplitude and duration (simulation results)

In Fig. 4, the detection threshold of nBBICS is $94 \mu A$ for $30.61 ps$ of current pulse duration. For the same current pulse duration, the detection threshold of double-access BBICS is $49 \mu A$ for $30.61 ps$ of current pulse duration. The double-access BBICS requires 48% less charge than the nBBICS to toggle.

C. Device under test

The double-access BBICS was embedded in a $40 nm$ STMicroelectronics CMOS test chip (with a core voltage of $1.2 V$). The BBICS was connected to a test element designed to mimic the kind of logic blocks a BBICS is supposed to monitor against SEEs. It consists of Nwells and Pwells shaped in a donut-like shape as depicted in the upper part of Fig. 5. The monitored area is $13 \mu m$ away from the BBICS to avoid any perturbation during acquisitions.

Each biasing contacts in the P+ areas (blue) and in the N+ areas (red) are respectively connected to the INPWELL and INNWELL of the BBICS. Our intent was to validate the complete detection by fully biasing the target through the BBICS.

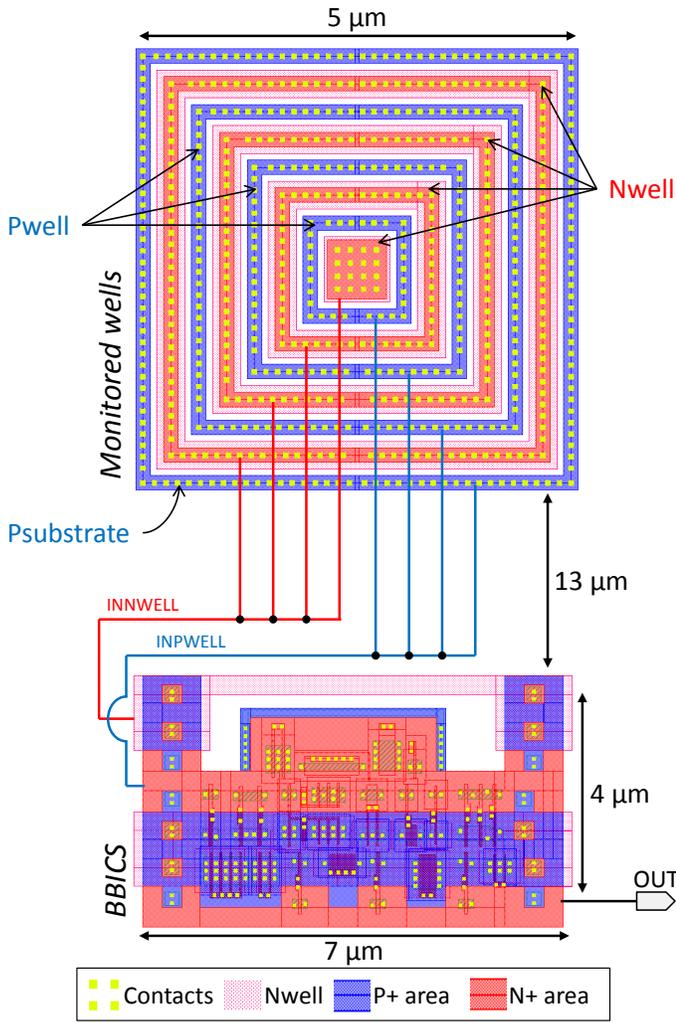


Fig. 5. Layout of double-access BBICS and layout of the monitored wells (not to scale)

IV. EXPERIMENTS

A. Experimental set-up

The laser source (Fig. 6) we used during our experiments produces laser pulses in the picosecond range. It has a 1030 nm wavelength, which makes it possible to access to the sensitive areas of a target through its backside. Our tests were actually performed through the target backside, which was thinned to 150 μm thickness to minimize the amount of power lost along the laser beam path. The laser beam was focused on the DUT's sensitive parts: given the $\times 100$ objective lens we used, we obtained a laser spot with a diameter of $\sim 1 \mu\text{m}$. Several laser pulse energies were chosen to have a full coverage area and evaluate the sensitivity maps.

To compare the BBICS results, Fig. 7 represents an SEU mapping from previous work [7] on a D Flip-Flop cell with exactly the same experimental settings. The measured SEU threshold energy was $0.5(\pm 0.1) \text{ nJ}$.

Mappings are performed by moving the backside microscope that injects the laser beam thanks to a XYZ stage (accurate to $0.1 \mu\text{m}$) whereas the wafer is stationary. At every

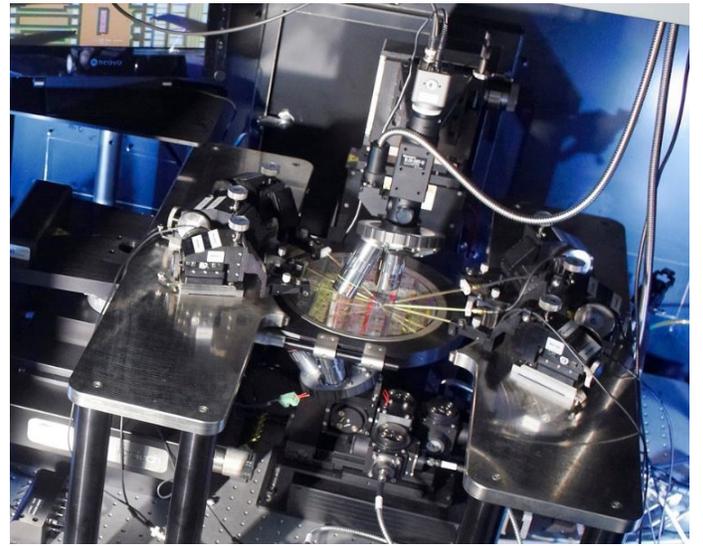


Fig. 6. Laser bench used for our experiments (injection through backside)

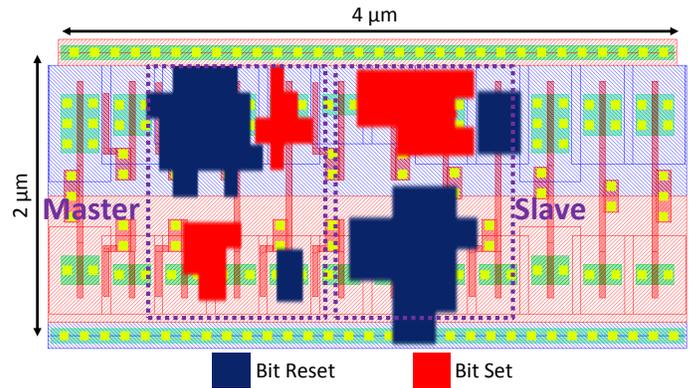


Fig. 7. Experimental results of a photoelectrical laser stimulation on a D Flip-Flop with a laser pulse duration of 30 ps and a laser energy of 0.7 nJ [7]

points, all the input signals are set with an FPGA, and the acquisitions are captured by a remote oscilloscope.

For our experiments, the main objective was to validate the efficiency of the double-access BBICS at detecting Single-Event Effects related currents close to the SEU threshold.

B. Experimental results (BBICS sensitivity maps)

Fig. 8 and Fig. 9 present detection sensitivity mappings of the double-access BBICS obtained while exposing the monitored element to laser pulses of 30 ps duration. These four detection maps were drawn respectively at 0.1 nJ, 0.2 nJ, 0.3 nJ and 0.4 nJ. Note that these energy levels correspond to the settings of our bench, the energy actually reaching the sensitive parts of the target is lower due to attenuation through the optical path and silicon.

At 0.1 nJ, the monitored area is fully covered: the laser-induced photocurrent has always triggered the BBICS alarm flag. At higher energies, the detection area extends largely

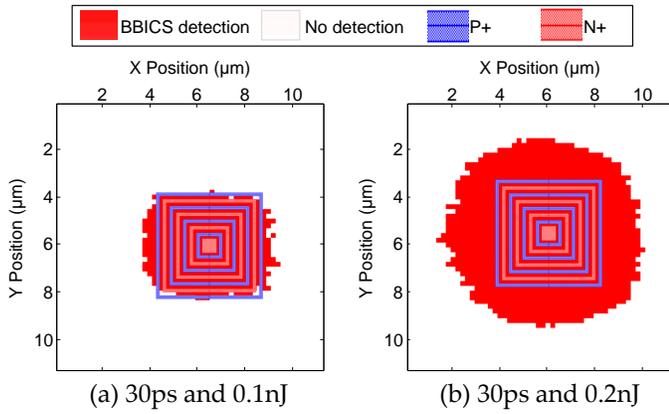


Fig. 8. BBICS laser detection maps on monitored wells at $0.1 nJ$ and $0.2 nJ$

outside the monitored element. At $0.4 nJ$, the detection area size is almost nine times than that of the monitored element.

The usefulness of BBICS is linked to their ability at detecting bulk currents with a magnitude lower than what is necessary to induce SEEs: i.e. no SEE in the monitored logic would escape detection. We validated the efficiency of the double-access BBICS on the basis of laser testing.

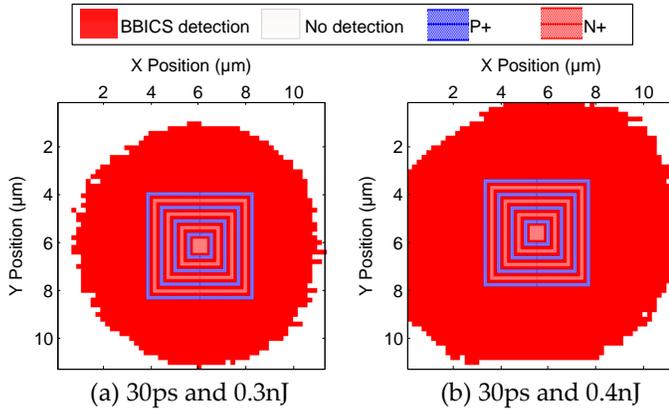


Fig. 9. BBICS laser detection maps on monitored wells at $0.3 nJ$ and $0.4 nJ$

As a result, practical laser experiments demonstrated a detection threshold of $0.1 nJ$ for BBICS design (at this energy the whole monitored area is covered) whereas the SEU threshold was higher at $0.5 nJ$. This is a promising evidence of the efficiency of double-access BBICS at detecting SEEs.

The SEE appearance is completely detected by the BBICS. The flag of the sensor may now be used to correct the error using different techniques of fault tolerance or resilience techniques [8–11].

V. CONCLUSION

This paper reports the first successful laser testing of a double-access BBICS embedded in an advanced technology node ($40 nm$ CMOS). We measured a $0.1 nJ$ detection threshold corresponding to a coverage of the whole BBICS monitored element. At higher energies, the detection area extends largely outside the monitored element. This detection threshold is

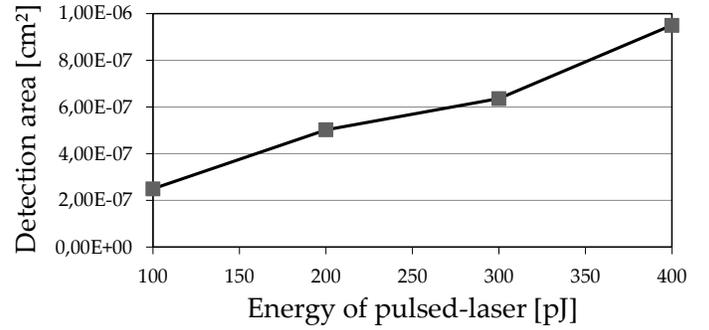


Fig. 10. Coverage area of BBICS detection with a laser pulse duration of $30 ps$

below the $0.5 nJ$ SEU threshold for a D Flip-Flop designed with the same process. This is a promising result that validates on experimental basis the efficiency of our BBICS design at detecting the occurrence of SEEs. The flag of the sensor may now be used to correct the error using different techniques of soft errors detection handling.

REFERENCES

- [1] B. Gill, M. Nicolaidis, F. Wolff, C. Papachristou, and S. Garverick, “An Efficient BICS Design for SEUs Detection and Correction in Semiconductor Memories,” *Design, Automation and Test in Europe Conference and Exhibition (DATE)*, 2005.
- [2] E. H. Neto, “Using Built-In Bulk Current to detect Soft Errors,” *18th Symposium on Integrated Circuits and Systems Design*, 2006.
- [3] E. H. Neto, F. L. Kastensmidt, and G. I. Wirth, “Tbulk-BICS : A Built-In Current Sensor Robust to Process and Temperature Variations for SET Detection,” *9th European Conference on Radiation and Its Effects on Components and Systems (RADECS)*, 2007.
- [4] A. Simionovski, G. Wirth, and S. Member, “Simulation Evaluation of an Implemented Set of Complementary Bulk Built-In Current Sensors With Dynamic Storage Cell,” *IEEE Transactions on Device and Materials Reliability*, 2014.
- [5] J. M. Dutertre, R. P. Bastos, O. Potin, M. L. Flottes, B. Rouzeyre, and G. D. Natale, “Improving the ability of Bulk Built-In Current Sensors to detect Single Event Effects by using triple-well CMOS,” *European Symposium on Reliability of Electron Devices, Failure Physics and Analysis (ESREF)*, 2014.
- [6] V. Pouget, H. Lapuyade, D. Lewis, Y. Deval, P. Fouillat, and L. Sarger, “SPICE Modeling of the Transient Response of Irradiated MOSFETs,” *IEEE Transactions on Nuclear Science*, 2000.
- [7] C. Champeix, N. Borrel, J.-M. Dutertre, B. Robisson, A. Sarafianos, and M. Lisart, “SEU sensitivity and modeling using picosecond pulsed laser stimulation of a D Flip-Flop in $40 nm$ CMOS technology,” *IEEE Defect and Fault Tolerance in VLSI and Nanotechnology Systems Symposium (DFTS)*, 2015.
- [8] R. Baumann, “Radiation-induced soft errors in advanced semiconductor technologies,” *IEEE Transactions on Device and Materials Reliability*, 2005.
- [9] W. Sootkaneeung and K. K. Saluja, “On Techniques for Handling Soft Errors in Digital Circuits,” *IEEE International Test Conference*, 2010.
- [10] P. Sawadpong, E. B. Allen, and J. B. Williams, “Exception Handling Defects: An Empirical Study,” *IEEE International Symposium on High-Assurance Systems Engineering*, 2012.
- [11] H. H. Zhu, “Handling Soft Error in Embedded Software for Networking System,” *IEEE International Symposium on Software Reliability Engineering Workshops*, 2014.